5036 N/B MAINTENANCE

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1. DEFINITION OF CONNECTORS & SWITCHES

MAIN BOARD(TOP SIDE)

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- J3 : FAX/MODEM/VOICE CARD CONNECTOR.
- J4 : EXTERNAL VGA MONITOR CONNECTOR.
- J5 : PARALLEL PORT CONNECTOR (PIO).
- J6 : SERIAL PORT CONNECTOR (SIO).
- J7 : USB PORT CONNECTOR.
- J8 : PORT REPLICATOR CONNECTOR.
- J9 : SYSTEM (CPU) FAN CONNECTOR.
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- J12 : INTERNAL RIGHT CHANNEL SPEAKER CONNECTOR.
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- J20 : INTERNAL MICROPHONE CONNECTOR.
- SW1 : SYSTEM POWER SWITCH.

MAIN BOARD(BOTTOM SIDE)

- J501 : 144 PIN 3.3V UNBUFFER DIMM SOCKET.
- J502 : PCCARD SLOT 2.
- J503 : PCCARD SLOT 1.
- J505 : SECONDARY IDE (CD-ROM) CONNECTOR.
- J506 : FLOPPY DISK DRIVE CONNECTOR.
- BT501 : CMOS BACK-UP BATTERY SOCKET.
- U506 : SYSTEM BIOS SOCKET.

AUDIO/CHARGER BOARD(TOP SIDE)

- J1 : TOUCHPAD BUTTON SWITCH CONNECTOR.
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AUDIO/CHARGER BOARD(BOTTOM SIDE)

- J501 : CONNECTOR TO CONNECT WITH MAIN BOARD.
- J502 : BATTERY PACK CONNECTOR.
- J503 : EXTERNAL SPEAKER CONNECTOR.
- J504 : EXTERNAL MICROPHONE CONNECTOR.

VGA BOARD(TOP SIDE)

- J2 : COVER SWITCH CONNECTOR.
- J3 : LVDS LCD PANEL TRANSLATION BOARD CONNECTOR.
- SW1 : SUSPEND RESUME BUTTON.

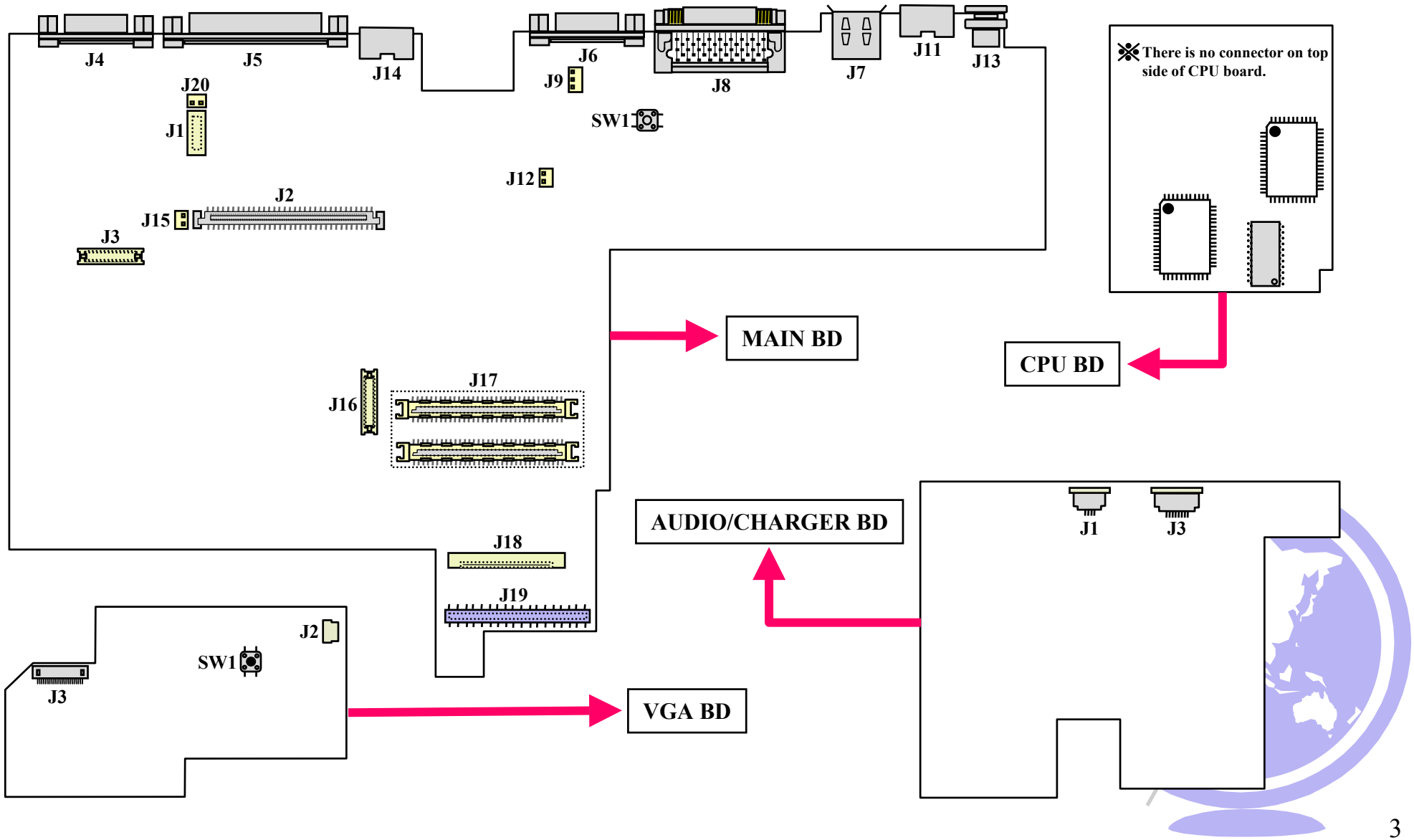
VGA BOARD(BOTTOM SIDE)

- J501 : CONNECTOR TO CONNECT WITH MAIN BOATD.

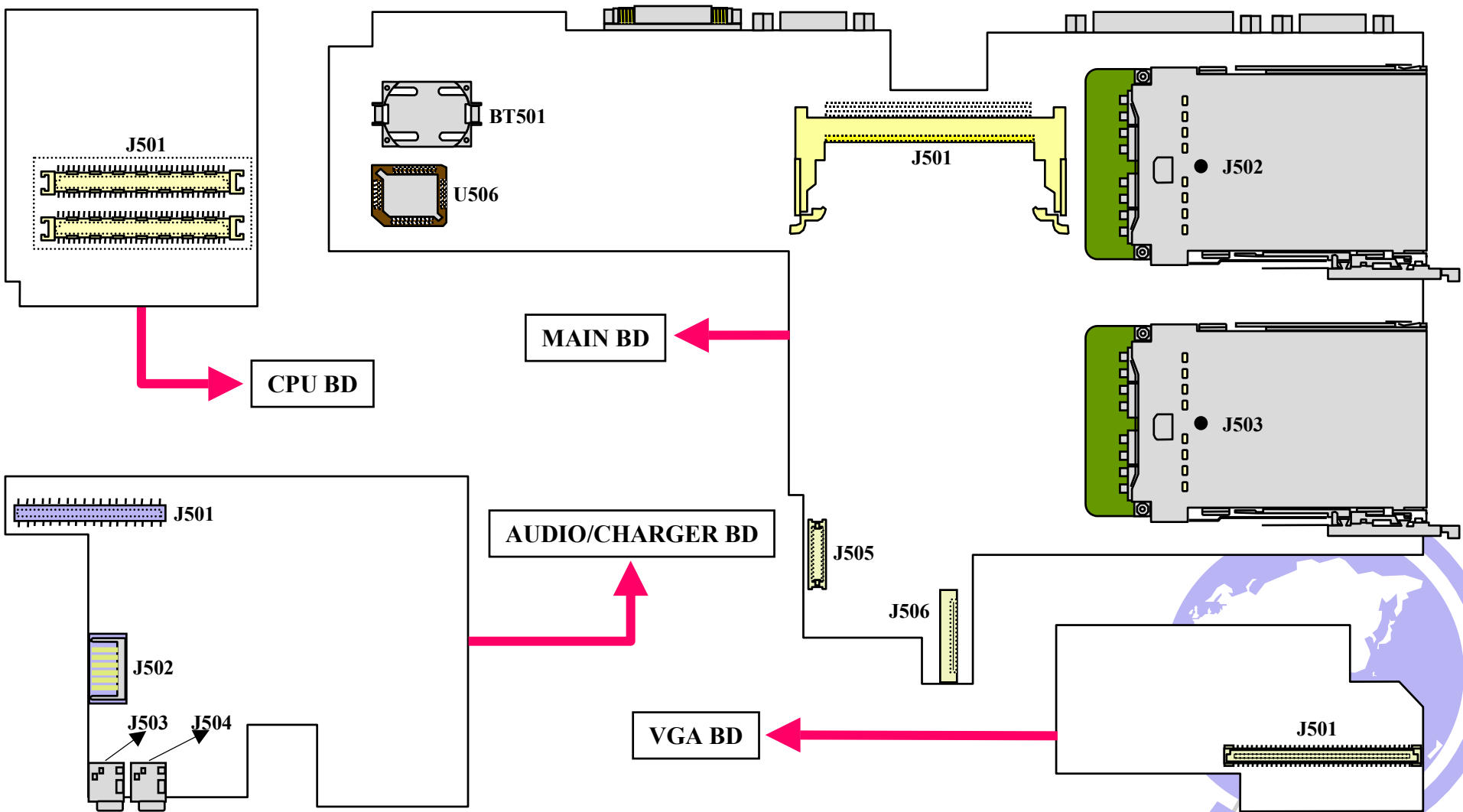
CPU BOARD(BOTTOM SIDE)

- J501 : CONNECTOR TO CONNECT WITH MAIN BOATD.

2 . LOCATION OF CONNECTORS & SWITCHES (TOP SIDE)



2 . LOCATION OF CONNECTORS & SWITCHES(BOTTOM SIDE)



3. MAJOR COMPONENTS

MAIN BOARD

- U1 : INTEL PIIX4 FW82371EB PCI/ISA BRIDGE.
- U5 : TI PCI1220PDV CARDBUS PCI-PCCARD CONTROLLER.
- U7 : MAX213 SIO DRIVE.
- U8, U504 : ON BOARD 32MB SDRAM. U9, U505
- U12 : HP FIR MODULE.
- U14 : INTEL MTXC FW82439TX PCI/ MEM/CACHE CONTROLLER.
- U506 : FLASHABLE SYSTEM BIOS.
- U507 : PC97338 SUPER I/O CONTROLLER.
- U509 : W48S67 CLOCK SYNTHESIZER.
- U510 : ESS ES9168S PCI AUDIO DRIVE.
- U511 : KEYBOARD CONTROLLER.
- J501 : EXPANSION DIMM MODULE.
- BT501 : CMOS BACK-UP BATTERY.

CPU BOARD

- U3, U4 : 512KB L2 CACHE.
- U5 : TAG SRAM.
- U501 : INTEL TILLAMOOK TCP CPU.

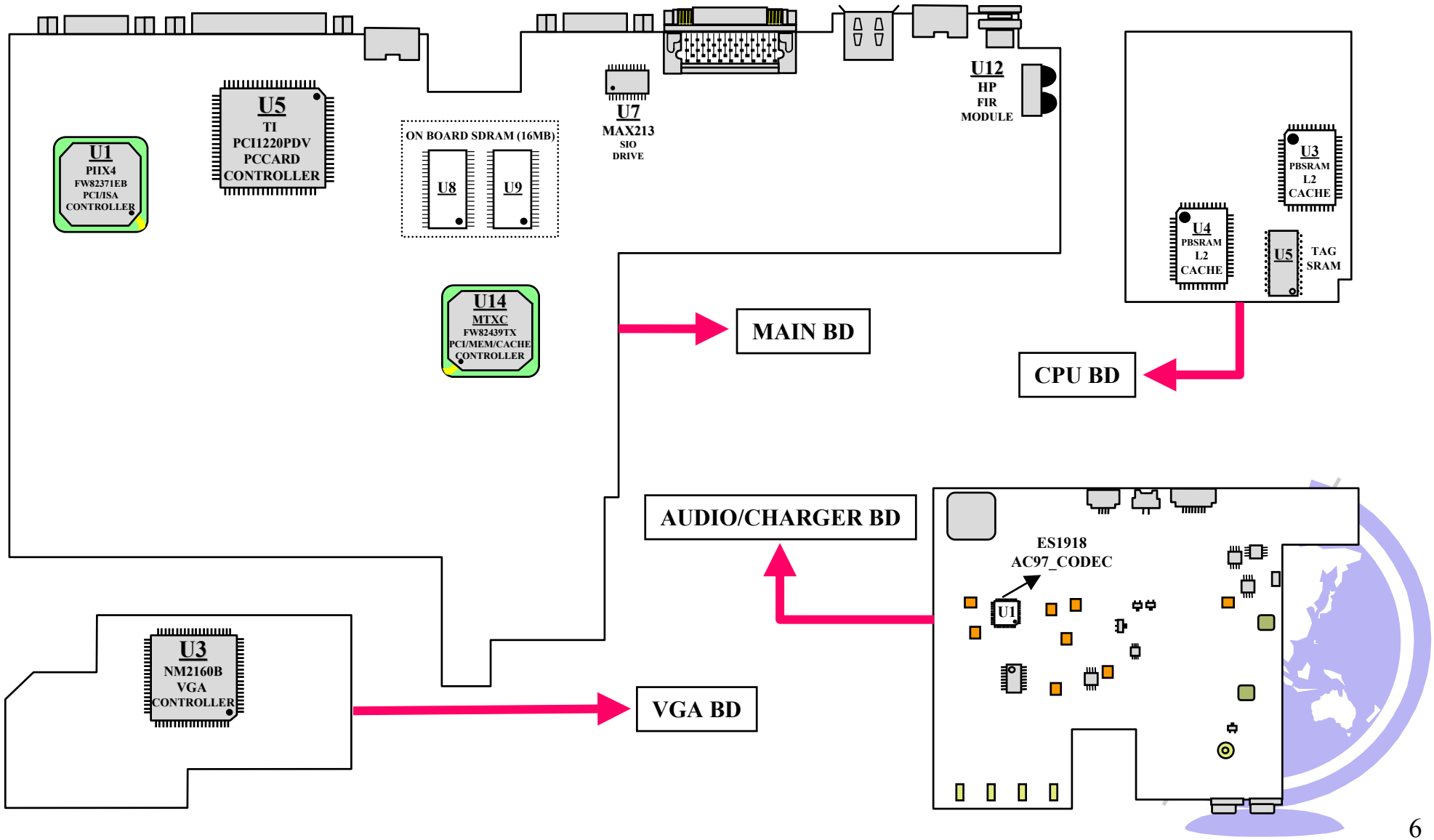
VGA BOARD

- U3 : NM2160B VGA CONTROLLER.

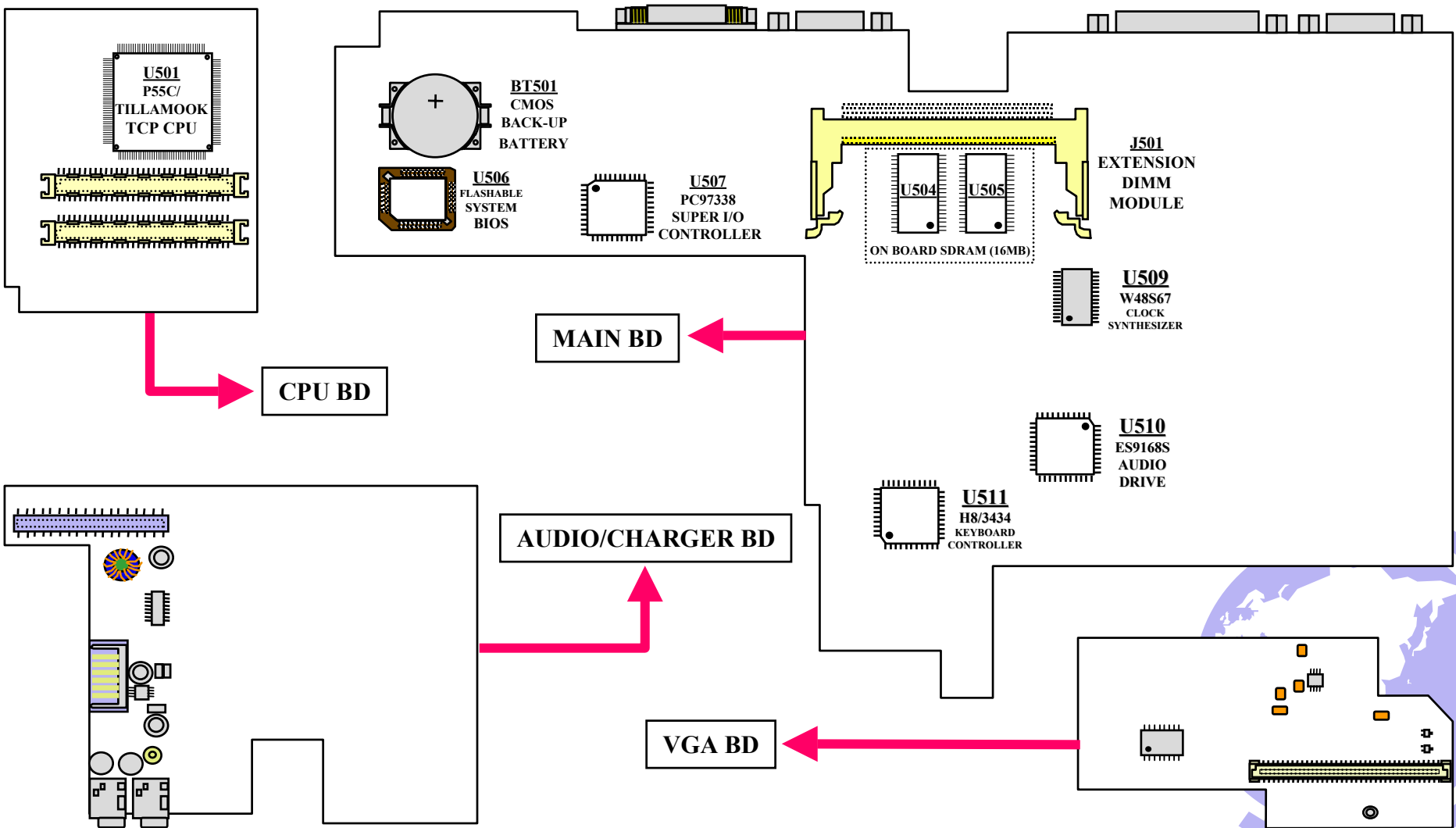
AUDIO/CHARGER BOARD

- U3 : ESS ES1918 AC97 CODEC.

4. LOCATION OF MAJOR COMPONENTS(TOP SIDE)



4. LOCATION OF MAJOR COMPONENTS(BOTTOM SIDE)



5. PIN DESCRIPTIONS OF MAJOR COMPONENTS

5.1 INTEL FW82439TX MEMORY/PCI/CACHE CONTROLLER (MTXC) (1) .

SYMBOL	TYPE	FUNCTION
A(31:1)	I/O	ADDRESS BUS. CONNECT TO THE ADDRESS BUS OF CPU.
BE(7:0)#	I	BYTE ENABLE.THE CPU BYTE ENABLES INDICATE WHICH BYTE LANE THE CURRENT CPU CYCLE IS ACCESSING.
ADS#	I	ADDRESS STATUS.THE CPU ASSERTS ADS# TO INDICATE THAT A NEW BUS CYCLE IS BEING DRIVEN.
BRDY#	O	BUS READY.THE TVX ASSERTS BRDY# TO INDICATES TO THE CPU THAT DATA IS AVAILABLE ON READS OR HAS BEEN RECEIVED ON WRITES.
NA#	O	NEXT ADDRESS.WHEN BURST SRAMS ARE USED IN THE SECOND LEVEL CACHE OR THE SECOND LEVEL CACHE IS DISABLE,THE TVX ASSERTS NA# IN T2 DURING CPU WRITE CYCLES AND WITH THE FIRST ASSERTION OF BRDY# DURING CPU LINE FILLS.
AHOLD	O	ADDRESS HOLD.THE TVX ASSERTS AHOLD WHEN A PCI INITIATOR IS PERFORMING A CYCLE TO DRAM.
EADS#	O	EXTERNAL ADDRESS STROBED.ASSERTS BY THE TVX TO REQUIRE THE FIRST LEVEL CACHE WHEN SERVICING PCI MASTER REFERENCES TO MAIN MEMORY.
BOFF#	O	BACK OFF.ASSERTS BY THE TVX WHEN REQUIRED TO TERMINATE A CPU CYCLE THAT WAS IN PROGRESS.
HITM#	I	HIT MODIFIED.ASSERTED BY THE CPU TO INDICATE THAT THE ADDRESS PRESENTED WITH THE LAST ASSERTION OF EADS# IS MODIFIED IN THE FIRST LEVEL CACHE AND NEED TO BE WRITTEN BACK.
M/ IO# D/ C# W/ R#	I	MEMORY/ IO;DATA/CONTROL;WRITE/READ.ASSERTS BY THE CPU TO INDICATE THE TYPE OF CYCLE THAT THE SYSTEM NEEDS TO PERFORM.
HLOCK#	I	HOST LOCK.ALL CPU CYCLES SAMPLED WITH THE ASSERTION OF HLOCK# AND ADS#,UNTIL THE NEGATION OF HLOCK# MUST BE ATOMIC.
CACHE#	I	CACHEABLE.ASSERTED BY THE CPU DURING A READ CYCLE TO INDICATE THE CPU WILL PERFORM A BURST LINE FILL.ASSERTED BY THE CPU DURING WRITE CYCLE TO INDICATE THE CPU WILL PERFORM A BURST WRITE-BACK CYCLE.

SYMBOL	TYPE	FUNCTION
KEN# / INV	I	CACHE ENABLE.KEN#/INV FUNCTIONS AS BOTH THE KEN# SIGNAL DURING CPU READ CYCLES,AND THE INV SIGNAL DURING L1 SNOOP CYCLES.
SMIACT#	I	SYSTEM MANAGEMENT INTERRUPT ACTIVE.SMIACT# IS ASSERTED BY THE CPU WHEN IT IS IN SYSTEM MANAGEMENT MODE AS A RESULT OF AN SMI.
RAS(5:0)#/ CS(5:0)#	O	ROW ADDRESS STROBE(EDO/SPM).THESE PINS SELECT THE DRAM ROW.CHIP SELECT(SDRAM).THESE PINS ACTIVATE THE SDRAM AND ACCEPT COMMAND WHEN IT IS LOW.
CAS(7:0)/ DQM(7:0)	O	COLUMN ADDRESS STROBE(EDO/SPM).THESE PINS SELECT WHICH BYTES ARE AFFECTED BY A DRAM CYCLE. INPUT/OUTPUT DATA MASK(SDRAM).THESE PINS ACT AS SYNCHRONIZED OUTPUT ENABLESDURING A READ CYCLE AND BYTE MASK DURING A WRITE CYCLE.
SRAS(B:A)#	O	SDRAM ROW ADDRESS STROBE(SDRAM). WHEN ACTIVE LOW THIS SIGNAL LATCHES ROW ADDRESS ON THE POSITIVE EDGE OF THE CLOCK. THIS SIGNAL ALSO ALLOWS ROW ACCESS AND PRE-CHARGE.
HD(63:0)	I/O	HOST DATA. THESE SIGNAL ARE CONNECTED TO HOST DATA BUS.
SCAS(B:A)#	O	SDRAM COLUMN ADDRSSS STROBE.SCAS(B:A)# LATCH COLUMN ADDRESS ON THE POSITIVE EDGE OF THE CLOCK WITH SCRAS(B:A)# LOW.THESE SIGNALS ENABLE COLUMN ACCESS.
MA(11:0)	O	MEMORY ADDRESS.
MWEB#	O	MEMORY WRITE ENABLE.MWE# SHOULD BE USED AS THE WRITE ENABLE PIN FOR THE MEMORY DATA BUS.
MWE#	O	MEMORY WRITE ENABLE.MWE# SHOULD BE USED AS THE WRITE ENABLE PIN FOR THE MEMORY DATA BUS.
CADV#/	O	CACE ADVANCE. ASSERTION CAUSES THE PBSRAM IN THE SECONDARY CACHE TO ADVANCE TO THE NEXT QWARD IN THE CACHE LINE.
CKE	O	SDRAM CLOCK ENABLE. WHEN THIS SIGNAL IS DIS-ASSERTED SDRAM ENTERS INTO POWER-DOWN MODE.

5.1 INTEL FW82439TX MEMORY/PCI/CACHE CONTROLLER (MTXC) (2) .

SYMBOL	TYPE	FUNCTION
CADS#/	O	CACHE ADDRESS STROBE. ASSERTION CAUSES THE PBSRAM IN THE SECONDARY CACHE TO LOAD THE PBSRAM ADDRESS REGISTER FROM THE PBSRAM ADDRESS PINS.
CKEB	O	SDRAM CLOCK ENABLE. WHEN THIS SIGNAL IS DE-ASSERTED SDRAM ENTERS POWER-DOWN MODE.
CCS#/	O	CACHE CHIP SELECT. THE SECONDARY LEVEL CACHE WILL POWER UP, AND PERFORM AN ACCESS IF THIS SIGNAL IS ASSERTED WHEN CADS# IS ASSERTED.
COE#	O	CACHE OUTPUT ENABLE.THE SECONDARY CACHE DATA RAMS DRIVE THE CPUS DATA BUS WHEN COE# IS ASSERTED
GWE#	O	GLOBAL WRITE ENABLE.WHEN THE L2 RAM TYPE IS PIPE-LINED BURST,GWE# ASSERTED CAUSES A QWORD TO BE WRITTEN INTO THE SECONDARY CACHE DATA RAMS IF THEY ARE POWERED UP.IT IS USED FOR L2 LINE FILLS.
BWE#/	O	BYTE WRITE ENABLE/CACHE GLOBAL CHIP SELECT.WHEN THE L2 RAM TYPE IS PIPELINED BURST,THIS PIN FUNCTI-ONS AS A BYTE WRITE ENABLE.WHEN THE L2 RAM TYPE IS STANDARD ASYNCHRONOUS RAMS,THIS PIN ACTS AS A GLOBAL CHIP SELECT.
TIO(7:0)	I/O	TAG ADDRESS.THESE ARE INTPUTS DURING CPU ACCESS AND OUTPUTS DURING SECOND LEVEL CACHE LINE FILLS AND THE SECOND LEVEL CACHE LINE INVALIDATES DUE TO INQUIRE CYCLES.
TWE#	O	TAG WRITE ENABLE.WHEN ASSERTED.NEW STATE AND TAG ADDRESSES ARE WRITTEN INTO THE EXTERNAL TAG.
AD(31:0)	I/O	ADDRESS DATA.THE STANDARD PCI ADDRESS AND DATA LINES.
C/BE(3:0)#	I/O	COMMAND/BYTE ENABLE.THE COMMAND IS DRIVEN WITH FRAME# ASSERTION,BYTE ENABLES CORRESPONDING TO SUPPLIED OR REQUESTED DATA IS DRIVEN ON FOLLOWI-NG CLOCKS.
FRAME#	I/O	FRAME.ASSERTION INDICATES THE ADDRESS PHASE OF PCI TRANSFER.
HCLKIN	I	HOST CLOCK IN.
PCLKIN	I	PCI CLOCK IN.
GNT3#/	O	PCI GRANT.PERMISSION IS GIVEN TO THE MASTER TO UED
DEVSEL#	I/O	DEVICE SELECT.THIS SIGNAL IS DRIVEN BY THE TVX WHEN A PCI INITIATOR IS ATTEMPTING TO ACCESS DRAM.
REQ(3:0)#	I	REQUEST.PCI MASTER REQUESTS FOR PCI.

SYMBOL	TYPE	FUNCTION
IRDY#	I/O	INITIATOR READY ASSERTED WHEN THE INITIATOR IS READY FOR DATA TRANSFER.
TRDY#	I/O	TARGET READY ASSERTED WHEN THE TARGET IS READY FOR A DATA TRANSFER.
STOP#	I/O	STOP.ASSERTED BY THE TARGET TO REQUEST THE MAST-ER TO STOP CURRENT TRANSACTION.
LOCK#	I/O	LOCK.UESD TO ESTABLISH, MAINTAIN,AND RELEASE RESOURCE LOCKS ON PCI.
KRQAK	I/O	KRQAK: THIS PIN IS USED WHEN A DRAM BASED CACHE TECHNOLOGY IS USED TO IMPLEMENT AN L2 CACHE. KRQAK IS A BI-DIRECTIONAL REFRESH REQUEST/ACKNOWLEDGE.
GNT(2:0)#	O	PCI GRANT.PERMISSION IS GIVEN TO THE MASTER TO UED PCI.
RST#	I	RESET: WHEN ASSERTED THIS SIGNAL WILL ASYNCHRONOUSLY RESET THE MTXC. THE PCI SIGNALS WILL ALSO TRI-STATE COMPLIANT TO PCI REV 2.0 AND 2.1 SPECIFICATION.
PHOLD#	I	PCI HOLD.THIS SIGNAL COMES FROM PIIX3.IT IS THE PII3 REQUEST FOR PCI.
PHLDA#	O	PCI HOLD ACKNOWLEDGE.THIS SIGNAL IS DRIVEN BY THE TVX TO GRANT PCI TO PIIX3.
PAR	I/O	PARITY.A SIGNAL PARITY BIT IS PROVIDED OVER AD(31:0) AND C/BE(3:0).
CLKRUN#	I/O	CLOCK RUN: AN OPEN DRAIN OUTPUT AND ALSO AN INPUT. MTXC REQUESTS THE ECNTRAL RESOURCE TO START, OR MAINTAIN THE PCI CLOCK BY THE ASSERTION OF CLKRUN#. MTXC WILL TRI-STATE CLKRUN# UPON DEASSERETION OF RESET.
TESTIN#	I	TEST IN: NAND-TREE MODE IS ACTIVATED BY DRIVING THIS PIN WHEN REQ# PINS ARE 0.
SUSCLK	I	SUSPEND CLOCK: 32KHZ INPUT FOR DRAM REFRESH CIRCUITY AND HIGH CLOCKING EVENTS IN SUSPEND STATE.
SUSTAT1#	I	SUSPEND STATE: SUS_STAT1 INDICATES MTXC'S POWER PLANE STATUS DURING SUSPEND MODE STATE.
VREF	3.3V OR 5V	VOLTAGE REFERENCE.
VCC	3.3V	MAIN VOLTAGE SUPPLY.
VCC(CPU)	3.3V OR 2.5V	CPU INTERFACE VOLTAGE SUPPLY.
VCC(SUS)	3.3V	SUSPEND WELL VOLTAGE SUPPLY: THESE PINS ARE THE PRIMARY VOLTAGE SUPPLY FOR THE MTXC SUSPEND LOGIC AND I/O.

5.2 INTEL 82371EB PCI-TO-ISA / IDE XCELERATOR (PIIX4) (1).

SIGNAL	TYPE	DESCRIPTION
AD[31:0]	I/O	**PCI ADDRESS/DATA.** AD[31:0] is a multiplexed address and data bus. During the first clock of a transaction, AD[31:0] contain a physical byte address (32 bits).During subsequent clocks, AD[31:0] contain data. A PIIX4 Bus transaction consists of an address phase followed by one or more data phases. Little-endian byte ordering is used. AD[7:0] define the least significant byte (LSB) and AD[31:24] the most significant byte (MSB). When PIIX4 is a Target, AD[31:0] are inputs during the address phase of a transaction. During the following data phase(s), PIIX4 may be asked to supply data on AD[31:0] for a PCI read, or accept data for a PCI write. As an Initiator, PIIX4 drives a valid address on AD[31:2] and 0 on AD[1:0] during the address phase, and drives write or latches read data on AD[31:0] during the data phase. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
C/BE#[3:0]	I/O	**BUS COMMAND AND BYTE ENABLES.** The command and byte enable signals are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase C/BE[3:0]# are used as Byte Enables. The Byte Enables determine which byte lanes carry meaningful data. C/BE0# applies to byte 0, C/BE1# to byte 1, etc. PIIX4 drives C/BE[3:0]# as an Initiator and monitors C/BE[3:0]# as a Target. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
CLKRUN#	I/O	**CLOCK RUN#.** This signal is used to communicate to PCI peripherals that the PCI clock will be stopped. Peripherals can assert CLKRUN# to request that the PCI clock be restarted or to keep it from stopping. This function follows the protocol described in the PCI Mobile Design Guide, Revision 1.0. **During Reset:** Low **After Reset:** Low **During POS:** High
DEVSEL#	I/O	**DEVICE SELECT.** PIIX4 asserts DEVSEL# to claim a PCI transaction through positive decoding or subtractive decoding (if enabled). As an output, PIIX4 asserts DEVSEL# when it samples IDSEL active in configuration cycles to PIIX4 configuration registers. PIIX4 also asserts DEVSEL# when an internal PIIX4 address is decoded or when PIIX4 subtractively or positively decodes a cycle for the ISA/EIO bus or IDE device. As an input, DEVSEL# indicates the response to a PIIX4 initiated transaction and is also sampled when deciding whether to subtractively decode the cycle. DEVSEL# is tri-stated from the leading edge of PCIRST#. DEVSEL# remains tri-stated until driven by PIIX4 as a target. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
FRAME#	I/O	**CYCLE FRAME.** FRAME# is driven by the current Initiator to indicate the beginning and duration of an access. While FRAME# is asserted data transfers continue. When FRAME# is negated the transaction is in the final data phase. FRAME# is an input to PIIX4 when it is the Target. FRAME# is an output when PIIX4 is the initiator. FRAME# remains tri-stated until driven by PIIX4 as an Initiator. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
IRDY#	I/O	**INITIATOR READY.** IRDY# indicates PIIX4□ ability, as an Initiator, to complete the current data phase of the transaction. It is used in conjunction with TRDY#. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates PIIX4 has valid data present on AD[31:0]. During a read, it indicates PIIX4 is prepared to latch data. IRDY# is an input to PIIX4 when PIIX4 is the Target and an output when PIIX4 is an Initiator. IRDY# remains tri-stated until driven by PIIX4 as a master.

SIGNAL	TYPE	DESCRIPTION
IDSEL	I	**INITIALIZATION DEVICE SELECT.** IDSEL is used as a chip select during PCI configuration read and write cycles. PIIX4 samples IDSEL during the address phase of a transaction. If IDSEL is sampled active, and the bus command is a configuration read or write, PIIX4 responds by asserting DEVSEL# on the next cycle. **PAR O CALCULATED PARITY SIGNAL.** PAR is □ven?parity and is calculated on 36 bits; AD[31:0] plus C/BE[3:0]#. □ven?parity means that the number of ?□ within the 36 bits plus PAR are counted and the sum is always even. PAR is always calculated on 36 bits regardless of the valid byte enables. PAR is generated for address and data phases and is only guaranteed to be valid one PCI clock after the corresponding address or data phase. PAR is driven and tri-stated identically to the AD[31:0] lines except that PAR is delayed by exactly one PCI clock. PAR is an output during the address phase (delayed one clock) for all PIIX4 initiated transactions. It is also an output during the data phase (delayed one clock) when PIIX4 is the Initiator of a PCI write transaction, and when it is the Target of a read transaction. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
PCIRST#	O	**PCI RESET.** PIIX4 asserts PCIRST# to reset devices that reside on the PCI bus. PIIX4 asserts PCIRST# during power-up and when a hard reset sequence is initiated through the RC register. PCIRST# is driven inactive a minimum of 1 ms after PWROK is driven active. PCIRST# is driven for a minimum of 1 ms when initiated through the RC register. PCIRST# is driven asynchronously relative to PCICLK. **During Reset:** Low **After Reset:** High **During POS:** High
PHOLD#	O	**PCI HOLD.** An active low assertion indicates that PIIX4 desires use of the PCI Bus. Once the PCI arbiter has asserted PHLDA# to PIIX4, it may not negate it until PHOLD# is negated by PIIX4. PIIX4 implements the passive release mechanism by toggling PHOLD# inactive for one PCICLK. **During Reset:** High-Z **After Reset:** High **During POS:** High
PHLDA#	I	**PCI HOLD ACKNOWLEDGE.** An active low assertion indicates that PIIX4 has been granted use of the PCI Bus. Once PHLDA# is asserted, it cannot be negated unless PHOLD# is negated first.
SERR#	I/O	**SYSTEM ERROR.** SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, PIIX4 can be programmed to generate a non-maskable interrupt (NMI) to the CPU. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
STOP#	I/O	**STOP.** STOP# indicates that PIIX4, as a Target, is requesting an initiator to stop the current transaction. As an Initiator, STOP# causes PIIX4 to stop the current transaction. STOP# is an output when PIIX4 is a Target and an input when PIIX4 is an Initiator. STOP# is tri-stated from the leading edge of PCIRST#. STOP# remains tri-stated until driven by PIIX4 as a slave. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
TRDY#	I/O	**TARGET READY.** TRDY# indicates PIIX4□ ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed when both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that PIIX4, as a Target, has place valid data on AD[31:0]. During a write, it indicates PIIX4, as a Target is prepared to latch data. TRDY# is an input to PIIX4 when PIIX4 is the Initiator and an output when PIIX4 is a Target. TRDY# is tri-stated from the leading edge of PCIRST#. TRDY# remains tri-stated until driven by PIIX4 as a slave. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z

5.2 INTEL 82371EB PCI-TO-ISA / IDE XCELERATOR (PIIX4) (2).

SIGNAL	TYPE	DESCRIPTION
AEN	O	**ADDRESS ENABLE.** AEN is asserted during DMA cycles to prevent I/O slaves from misinterpreting DMA cycles as valid I/O cycles. When negated, AEN indicates that an I/O slave may respond to address and I/O commands. When asserted, AEN informs I/O resources on the ISA bus that a DMA transfer is occurring. This signal is also driven high during PIIX4 initiated refresh cycles. **During Reset:** High-Z **After Reset:** Low **During POS:** Low
BALE	O	**BUS ADDRESS LATCH ENABLE.** BALE is asserted by PIIX4 to indicate that the address (SA[19:0], LA[23:17]) and SBHE# signal lines are valid. The LA[23:17] address lines are latched on the trailing edge of BALE. BALE remains asserted throughout DMA and ISA master cycles. **During Reset:** High-Z **After Reset:** Low **During POS:** Low
IOCHK#/ GPI0	I	**I/O CHANNEL CHECK.** IOCHK# can be driven by any resource on the ISA bus. When asserted, it indicates that a parity or an uncorrectable error has occurred for a device or memory on the ISA bus. A NMI will be generated to the CPU if the NMI generation is enabled. If the EIO bus is used, this signal becomes a general purpose input.
IOCHRDY	I/O	**I/O CHANNEL READY.** Resources on the ISA Bus negate IOCHRDY to indicate that wait states are required to complete the cycle. This signal is normally high. IOCHRDY is an input when PIIX4 owns the ISA Bus and the CPU or a PCI agent is accessing an ISA slave, or during DMA transfers. IOCHRDY is output when an external ISA Bus Master owns the ISA Bus and is accessing DRAM or a PIIX4 register. As a PIIX4 output, IOCHRDY is driven inactive (low) from the falling edge of the ISA commands. After data is available for an ISA master read or PIIX4 latches the data for a write cycle, IOCHRDY is asserted for 70 ns. After 70 ns, PIIX4 floats IOCHRDY. The 70 ns includes both the drive time and the time it takes PIIX4 to float IOCHRDY. PIIX4 does not drive this signal when an ISA Bus master is accessing an ISA Bus slave. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
IOCS16#	I	**16-BIT I/O CHIP SELECT.** This signal is driven by I/O devices on the ISA Bus to indicate support for 16-bit I/O bus cycles.
IOR#	I/O	**I/O READ.** IOR# is the command to an ISA I/O slave device that the slave may drive data on to the ISA data bus (SD[15:0]). The I/O slave device must hold the data valid until after IOR# is negated. IOR# is an output when PIIX4 owns the ISA Bus. IOR# is an input when an external ISA master owns the ISA Bus. **During Reset:** High-Z **After Reset:** High **During POS:** High
IOW#	I/O	**I/O WRITE.** IOW# is the command to an ISA I/O slave device that the slave may latch data from the ISA data bus (SD[15:0]). IOW# is an output when PIIX4 owns the ISA Bus. IOW# is an input when an external ISA master owns the ISA Bus. **During Reset:** High-Z **After Reset:** High **During POS:** High
LA[23:17]/ GPO[7:1]	I/O	**ISA LA[23:17].** LA[23:17] address lines allow accesses to physical memory on the ISA Bus up to 16 Mbytes. LA[23:17] are outputs when PIIX4 owns the ISA Bus. The LA[23:17] lines become inputs whenever an ISA master owns the ISA Bus. If the EIO bus is used, these signals become a general purpose output. **During Reset:** High-Z **After Reset:** Undefined **During POS:** Last LA/GPO
MEMCS16#	I/O	**MEMORY CHIP SELECT 16.** MEMCS16# is a decode of LA[23:17] without any qualification of the command signal lines. ISA slaves that are 16-bit memory devices drive this signal low. PIIX4 ignores MEMCS16# during I/O access cycles and refresh cycles. MEMCS16# is an input when PIIX4 owns the ISA Bus. PIIX4 drives this signal low during ISA master to PCI memory cycles.

SIGNAL	TYPE	DESCRIPTION
MEMR#	I/O	**MEMORY READ.** MEMR# is the command to a memory slave that it may drive data onto the ISA data bus. MEMR# is an output when PIIX4 is a master on the ISA Bus. MEMR# is an input when an ISA master, other than PIIX4, owns the ISA Bus. This signal is also driven by PIIX4 during refresh cycles. For DMA cycles, PIIX4, as a master, asserts MEMR#. **During Reset:** High-Z **After Reset:** High **During POS:** High
MEMW#	I/O	**MEMORY WRITE.** MEMW# is the command to a memory slave that it may latch data from the ISA data bus. MEMW# is an output when PIIX4 owns the ISA Bus. MEMW# is an input when an ISA master, other than PIIX4, owns the ISA Bus. For DMA cycles, PIIX4, as a master, asserts MEMW#. **During Reset:** High-Z **After Reset:** High **During POS:** High
REFRESH#	I/O	**REFRESH.** As an output, REFRESH# is used by PIIX4 to indicate when a refresh cycle is in progress. It should be used to enable the SA[7:0] address to the row address inputs of all banks of dynamic memory on the ISA Bus. Thus, when MEMR# is asserted, the entire expansion bus dynamic memory is refreshed. Memory slaves must not drive any data onto the bus during refresh. As an output, this signal is driven directly onto the ISA Bus. This signal is an output only when PIIX4 DMA refresh controller is a master on the bus responding to an internally generated request for refresh. As an input, REFRESH# is driven by 16-bit ISA Bus masters to initiate refresh cycles. **During Reset:** High-Z **After Reset:** High **During POS:** High
RSTDRV	O	**RESET DRIVE.** PIIX4 asserts RSTDRV to reset devices that reside on the ISA/EIO Bus. PIIX4 asserts this signal during a hard reset and during power-up. RSTDRV is asserted during power-up and negated after PWROK is driven active. RSTDRV is also driven active for a minimum of 1 ms if a hard reset has been programmed in the RC register. **During Reset:** High **After Reset:** Low **During POS:** Low
SA[19:0]	I/O	**SYSTEM ADDRESS[19:0].** These bi-directional address lines define the selection with the granularity of 1 byte within the 1-Megabyte section of memory defined by the LA[23:17] address lines. The address lines SA[19:17] that are coincident with LA[19:17] are defined to have the same values as LA[19:17] for all memory cycles. For I/O accesses, only SA[15:0] are used, and SA[19:16] are undefined. SA[19:0] are outputs when PIIX4 owns the ISA Bus. SA[19:0] are inputs when an external ISA Master owns the ISA Bus. **During Reset:** High-Z **After Reset:** Undefined **During POS:** Last SA
SBHE#	I/O	**SYSTEM BYTE HIGH ENABLE.** SBHE# indicates, when asserted, that a byte is being transferred on the upper byte (SD[15:8]) of the data bus. SBHE# is negated during refresh cycles. SBHE# is an output when PIIX4 owns the ISA Bus. SBHE# is an input when an external ISA master owns the ISA Bus. **During Reset:** High-Z **After Reset:** Undefined **During POS:** High
SD[15:0]	I/O	**SYSTEM DATA.** SD[15:0] provide the 16-bit data path for devices residing on the ISA Bus. SD[15:8] correspond to the high order byte and SD[7:0] correspond to the low order byte. SD[15:0] are undefined during refresh. **During Reset:** High-Z **After Reset:** Undefined **During POS:** High-Z
SMEMR#	O	**STANDARD MEMORY READ.** PIIX4 asserts SMEMR# to request an ISA memory slave to drive data onto the data lines. If the access is below the 1-Mbyte range (00000000h?00FFFFFh) during DMA compatible, PIIX4 master, or ISA master cycles, PIIX4 asserts SMEMR#. SMEMR# is a delayed version of MEMR#.

5.2 INTEL 82371EB PCI-TO-ISA / IDE XCELERATOR (PIIX4) (3).

SIGNAL	TYPE	DESCRIPTION
SMEMW#	O	**STANDARD MEMORY WRITE.** PIIX4 asserts SMEMW# to request an ISA memory slave to accept data from the data lines. If the access is below the 1-Mbyte range (00000000h?00FFFFFh) during DMA compatible, PIIX4 master, or ISA master cycles, PIIX4 asserts SMEMW#. SMEMW# is a delayed version of MEMW#. **During Reset:** High-Z **After Reset:** High **During POS:** High
ZEROWS#	I	**ZERO WAIT STATES.** An ISA slave asserts ZEROWS# after its address and command signals have been decoded to indicate that the current cycle can be shortened. A 16-bit ISA memory cycle can be reduced to two SYSCLKs. An 8-bit memory or I/O cycle can be reduced to three SYSCLKs. ZEROWS# has no effect during 16-bit I/O cycles. If IOCHRDY is negated and ZEROWS# is asserted during the same clock, then ZEROWS# is ignored and wait states are added as a function of IOCHRDY.
A20GATE	I	**ADDRESS 20 GATE.** This input from the keyboard controller is logically combined with bit 1 (FAST_A20) of the Port 92 Register, which is then output via the A20M# signal.
BIOSCS#	O	**BIOS CHIP SELECT.** This chip select is driven active during read or write accesses to enabled BIOS memory ranges. BIOSCS# is driven combinatorially from the ISA addresses SA[16:0] and LA[23:17], except during DMA cycles. During DMA cycles, BIOSCS# is not generated. **During Reset:** High **After Reset:** High **During POS:** High
KBCCS#/ GPO26	O	**KEYBOARD CONTROLLER CHIP SELECT.** KBCCS# is asserted during I/O read or write accesses to KBC locations 60h and 64h. It is driven combinatorially from the ISA addresses SA[19:0] and LA[23:17]. If the keyboard controller does not require a separate chip select, this signal can be programmed to a general purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO
MCCS#	O	**MICROCONTROLLER CHIP SELECT.** MCCS# is asserted during I/O read or write accesses to IO locations 62h and 66h. It is driven combinatorially from the ISA addresses SA[19:0] and LA[23:17]. **During Reset:** High **After Reset:** High **During POS:** High
PCS0# PCS1#	O	**PROGRAMMABLE CHIP SELECTS.** These active low chip selects are asserted for ISA I/O cycles which are generated by PCI masters and which hit the programmable I/O ranges defined in the Power Management section. The X-Bus buffer signals (XOE# and XDIR#) are enabled while the chip select is active. (i.e., it is assumed that the peripheral which is selected via this pin resides on the X-Bus.) **During Reset:** High **After Reset:** High **During POS:** High
RCIN#	I	**RESET CPU.** This signal from the keyboard controller is used to generate an INIT signal to the CPU.
RTCALE/ GPO25	O	**REAL TIME CLOCK ADDRESS LATCH ENABLE.** RTCALE is used to latch the appropriate memory address into the RTC. A write to port 70h with the appropriate RTC memory address that will be written to or read from causes RTCALE to be asserted. RTCALE is asserted on falling IOW# and remains asserted for two SYSCLKs. If the internal Real Time Clock is used, this signal can be programmed as a general purpose output.
RTCCS#/ GPO24	O	**REAL TIME CLOCK CHIP SELECT.** RTCCS# is asserted during read or write I/O accesses to RTC location 71h. RTCCS# can be tied to a pair of external OR gates to generate the real time clock read and write command signals. If the internal Real Time Clock is used, this signal can be programmed as a general purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO

SIGNAL	TYPE	DESCRIPTION
XDIR#/ GPO22	O	**X-BUS TRANSCEIVER DIRECTION.** XDIR# is tied directly to the direction control of a 74?45 that buffers the X-Bus data, XD[7:0]. XDIR# is asserted (driven low) for all I/O read cycles regardless if the accesses is to a PIIX4 supported device. XDIR# is asserted for memory cycles only if BIOS or APIC space has been decoded. For PCI master initiated read cycles, XDIR# is asserted from the falling edge of either IOR# or MEMR# (from MEMR# only if BIOS or APIC space has been decoded), depending on the cycle type. For ISA master-initiated read cycles, XDIR# is asserted from the falling edge of either IOR# or MEMR# (from MEMR# only if BIOS space has been decoded), depending on the cycle type. When the rising edge of IOR# or MEMR# occurs, PIIX4 negates XDIR#. For DMA read cycles from the X-Bus, XDIR# is driven low from DACKx# falling and negated from DACKx# rising. At all other times, XDIR# is negated high. If the X-Bus not used, then this signal can be programmed to be a general purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO
XOE#/ GPO23	O	**X-BUS TRANSCEIVER OUTPUT ENABLE.** XOE# is tied directly to the output enable of a 74?45 that buffers the X-Bus data, XD[7:0], from the system data bus, SD[7:0]. XOE# is asserted anytime a PIIX4 supported X-Bus device is decoded, and the devices decode is enabled in the X-Bus Chip Select Enable Register (BIOSCS#, KBCCS#, RTCCS#, MCCS#) or the Device Resource B (PCCS0#) and Device Resource C (PCCS1#). XOE# is asserted from the falling edge of the ISA commands (IOR#, IOW#, MEMR#, or MEMW#) for PCI Master and ISA master-initiated cycles. XOE# is negated from the rising edge of the ISA command signals for PCI Master initiated cycles and the SA[16:0] and LA[23:17] address for ISA master-initiated cycles. XOE# is not generated during any access to an X-Bus-peripheral in which its decode space has been disabled. If an X-Bus not used, then this signal can be programmed to be a general purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO
DACK[0,1,2,3]# DACK[5,6,7]#	O	**DMA ACKNOWLEDGE.** The DACK# output lines indicate that a request for DMA service has been granted by PIIX4 or that a 16-bit master has been granted the bus. The active level (high or low) is programmed via the DMA Command Register. These lines should be used to decode the DMA slave device with the IOR# or IOW# line to indicate selection. If used to signal acceptance of a bus master request, this signal indicates when it is legal to assert MASTER#. If the DREQ goes inactive prior to DACK# being asserted, the DACK# signal will not be asserted. **During Reset:** High **After Reset:** High **During POS:** High
DREQ[0,1,2,3] DREQ[5,6,7]	I	**DMA REQUEST.** The DREQ lines are used to request DMA service from PIIX4 DMA controller or for a 16-bit master to gain control of the ISA expansion bus. The active level (high or low) is programmed via the DMA Command Register. All inactive to active edges of DREQ are assumed to be asynchronous. The request must remain active until the appropriate DACKx# signal is asserted.
REQ[A:C]#/ GPI[2:4]	I	**PC/PCI DMA REQUEST.** These signals are the DMA requests for PC/PCI protocol. They are used by a PCI agent to request DMA services and follow the PCI Expansion Channel Passing protocol as defined in the *PCI DMA* section. If the PC/PCI request is not needed, these pins can be used as general-purpose inputs.

5.2 INTEL 82371EB PCI-TO-ISA / IDE XCELERATOR (PIIX4) (4).

SIGNAL	TYPE	DESCRIPTION
GNT[A:C]#/ GPO[9:11]	O	**PC/PCI DMA ACKNOWLEDGE.** These signals are the DMA grants for PC/PCI protocol. They are used by a PIIX4 to acknowledge DMA services and follow the PCI Expansion Channel Passing protocol as defined in the *PCI DMA* section. If the PC/PCI request is not needed, these pins can be used as general-purpose outputs. **During Reset:** High **After Reset:** High **During POS:** High/GPO
TC	O	**TERMINAL COUNT.** PIIX4 asserts TC to DMA slaves as a terminal count indicator. PIIX4 asserts TC after a new address has been output, if the byte count expires with that transfer. TC remains asserted until AEN is negated, unless AEN is negated during an autoinitialization. TC is negated before AEN is negated during an autoinitialization. **During Reset:** Low **After Reset:** Low **During POS:** Low
APICACK#/ GPO12	O	**APIC ACKNOWLEDGE.** This active low output signal is asserted by PIIX4 after its internal buffers are flushed in response to the APICREQ# signal. When the I/O APIC samples this signal asserted it knows that PIIX4 buffers are flushed and that it can proceed to send the APIC interrupt. The APICACK# output is synchronous to PCICLK. If the external APIC is not used, then this is a general-purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO
APICCS#/ GPO13	O	**APIC CHIP SELECT.** This active low output signal is asserted when the APIC Chip Select is enabled and a PCI originated cycle is positively decoded within the programmed I/O APIC address space. If the external APIC is not used, this pin is a general-purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO
APICREQ#/ GPI5	I	**APIC REQUEST.** This active low input signal is asserted by an external APIC device prior to sending an interrupt over the APIC serial bus. When PIIX4 samples this pin active it will flush its F-type DMA buffers pointing towards PCI. Once the buffers are flushed, PIIX4 asserts APICACK# which indicates to the external APIC that it can proceed to send the APIC interrupt. The APICREQ# input must be synchronous to PCICLK. If the external APIC is not used, this pin is a general-purpose input. **INTR** OD **INTERRUPT.** See CPU Interface Signals.
IRQ0/ GPO14	O	**INTERRUPT REQUEST 0.** This output reflects the state of the internal IRQ0 signal from the system timer. If the external APIC is not used, this pin is a general-purpose output. **During Reset:** Low **After Reset:** Low **During POS:** IRQ0/GPO **IRQ1** I **INTERRUPT REQUEST 1.** IRQ1 is always edge triggered and can not be modified by software to level sensitive. A low to high transition on IRQ1 is latched by PIIX4. IRQ1 must remain asserted until after the interrupt is acknowledged. If the input goes inactive before this time, a default IRQ7 is reported in response to the interrupt acknowledge cycle.
IRQ 3:7, 9:11,14:15	I	**INTERRUPT REQUESTS 3:7, 9:11, 14:15.** The IRQ signals provide both system board components and ISA Bus I/O devices with a mechanism for asynchronously interrupting the CPU. These interrupts may be programmed for either an edge sensitive or a high level sensitive assertion mode. Edge sensitive is the default configuration.An active IRQ input must remain asserted until after the interrupt is acknowledged. If the input goes inactive before this time, a default IRQ7 is reported in response to the interrupt acknowledge cycle.

SIGNAL	TYPE	DESCRIPTION
IRQ8#/ GPI6	I/O	**IRQ 8#.** IRQ8# is always an active low edge triggered interrupt and can not be modified by software. IRQ8# must remain asserted until after the interrupt is acknowledged. If the input goes inactive before this time, a default IRQ7 is reported in response to the interrupt acknowledge cycle. If using the internal RTC, then this can be programmed as a general-purpose input. If enabling an APIC, this signal becomes an output and must not be programmed as a general purpose input.
IRQ9OUT#/ GPO29	O	**IRQ9OUT#.** IRQ9OUT# is used to route the internally generated SCI and SMBus interrupts out of the PIIX4 for connection to an external IO APIC. If APIC is disabled, this signal pin is a General Purpose Output. **During Reset:** High **After Reset:** High **During POS:** IRQ9OUT#/GPO
IRQ 12/M	I	**INTERRUPT REQUEST 12.** In addition to providing the standard interrupt function as described in the pin description for IRQ[3:7,9:11,14:15], this pin can also be programmed to provide the mouse interrupt function. When the mouse interrupt function is selected, a low to high transition on this signal is latched by PIIX4 and an INTR is generated to the CPU as IRQ12. An internal IRQ12 interrupt continues to be generated until a Reset or an I/O read access to address 60h (falling edge of IOR#) is detected.
PIRQ[A:D]#	I/OD PCI	**PROGRAMMABLE INTERRUPT REQUEST.** The PIRQx# signals are active low, level sensitive, shareable interrupt inputs. They can be individually steered to ISA interrupts IRQ [3:7,9:12,14:15]. The USB controller uses PIRQD# as its output signal.
SERIRQ/ GPI7	I/O	**SERIAL INTERRUPT REQUEST.** Serial interrupt input decoder, typically used in conjunction with the Distributed DMA protocol. If not using serial interrupts, this pin can be used as a general-purpose input.
A20M#	OD	**ADDRESS 20 MASK.** PIIX4 asserts A20M# to the CPU based on combination of Port 92 Register, bit 1 (FAST_A20), and A20GATE input signal. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
CPURST	OD	**CPU RESET.** PIIX4 asserts CPURST to reset the CPU. PIIX4 asserts CPURST during power-up and when a hard reset sequence is initiated through the RC register. CPURST is driven inactive a minimum of 2 ms after PWROK is driven active. CPURST is driven active for a minimum of 2 ms when initiated through the RC register. The inactive edge of CPURST is driven synchronously to the rising edge of PCICLK. If a hard reset is initiated through the RC register, PIIX4 resets its internal registers (in both core and suspend wells) to their default state. This signal is active high for Pentium processor and active-low for Pentium II processor as determined by CONFIG1 signal. For values **During Reset**, **After Reset**, and **During POS**, see the *Suspend/Resume and Resume Control Signaling* section.
FERR#	I	**NUMERIC COPROCESSOR ERROR.** This pin functions as a FERR# signal supporting coprocessor errors. This signal is tied to the coprocessor error signal on the CPU. If FERR# is asserted, PIIX4 generates an internal IRQ13 to its interrupt controller unit. PIIX4 then asserts the INT output to the CPU. FERR# is also used to gate the IGNNE# signal to ensure that IGNNE# is not asserted to the CPU unless FERR# is active.
SLP#	OD	**SLEEP.** This signal is output to the Pentium II processor in order to put it into Sleep state. For Pentium processor it is a No Connect.

5.2 INTEL 82371EB PCI-TO-ISA / IDE XCELERATOR (PIIX4) (5).

SIGNAL	TYPE	DESCRIPTION
IGNNE#	OD	**IGNORE NUMERIC EXCEPTION.** This signal is connected to the ignore numeric exception pin on the CPU. IGNNE# is only used if the PIIX4 coprocessor error reporting function is enabled. If FERR# is active, indicating a coprocessor error, a write to the Coprocessor Error Register (F0h) causes the IGNNE# to be asserted. IGNNE# remains asserted until FERR# is negated. If FERR# is not asserted when the Coprocessor Error Register is written, the IGNNE# signal is not asserted. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
INIT	OD	**INITIALIZATION.** INIT is asserted in response to any one of the following conditions. When the System Reset bit in the Reset Control Register is reset to 0 and the Reset CPU bit toggles from 0 to 1, PIIX4 initiates a soft reset by asserting INIT. PIIX4 also asserts INIT if a Shut Down Special cycle is decoded on the PCI Bus, if the RCIN# signal is asserted, or if a write occurs to Port 92h, bit 0. When asserted, INIT remains asserted for approximately 64 PCI clocks before being negated. This signal is active high for Pentium processor and active-low for Pentium II processor as determined by CONFIG1 signal. **Pentium Processor:** **During Reset:** Low **After Reset:** Low **During POS:** Low **Pentium II Processor:** **During Reset:** High **After Reset:** High **During POS:** High
INTR	OD	**CPU INTERRUPT.** INTR is driven by PIIX4 to signal the CPU that an interrupt request is pending and needs to be serviced. It is asynchronous with respect to SYSCLK or PCICLK and is always an output. The interrupt controller must be programmed following PCIRST# to ensure that INTR is at a known state. **During Reset:** Low **After Reset:** Low **During POS:** Low
NMI	OD	**NON-MASKABLE INTERRUPT.** NMI is used to force a nonmaskable interrupt to the CPU. PIIX4 generates an NMI when either SERR# or IOCHK# is asserted, depending on how the NMI Status and Control Register is programmed. The CPU detects an NMI when it detects a rising edge on NMI. After the NMI interrupt routine processes the interrupt, the NMI status bits in the NMI Status and Control Register are cleared by software. The NMI interrupt routine must read this register to determine the source of the interrupt. The NMI is reset by setting the corresponding NMI source enable/disable bit in the NMI Status and Control Register. To enable NMI interrupts, the two NMI enable/disable bits in the register must be set to 0, and the NMI mask bit in the NMI Enable/Disable and Real Time Clock Address Register must be set to 0. Upon PCIRST#, this signal is driven low. **During Reset:** Low **After Reset:** Low **During POS:** Low
SMI#	OD	**SYSTEM MANAGEMENT INTERRUPT.** SMI# is an active low synchronous output that is asserted by PIIX4 in response to one of many enabled hardware or software events. The CPU recognizes the falling edge of SMI# as the highest priority interrupt in the system, with the exception of INIT, CPURST, and FLUSH. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
STPCLK#	OD	**STOP CLOCK.** STPCLK# is an active low synchronous output that is asserted by PIIX4 in response to one of many hardware or software events. STPCLK# connects directly to the CPU and is synchronous to PCICLK. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-
RTCX1, RTCX2	I/O	**RTC CRYSTAL INPUTS:** These connected directly to a 32.768-kHz crystal. External capacitors are required. These clock inputs are required even if the internal RTC is not being used.

SIGNAL	TYPE	DESCRIPTION
CLK48	I	**48-MHZ CLOCK.** 48-MHz clock used by the internal USB host controller. This signal may be stopped during suspend modes.
PCICLK	I	**FREE-RUNNING PCI CLOCK.** A clock signal running at 30 or 33 MHz, PCICLK provides timing for all transactions on the PCI Bus. All other PCI signals are sampled on the rising edge of PCICLK, and all timing parameters are defined with respect to this edge. Because many of the circuits in PIIX4 run off the PCI clock, this signal MUST be kept active, even if the PCI bus clock is not active.
OSC	I	**14.31818-MHZ CLOCK.** Clock signal used by the internal 8254 timer. This clock signal may be stopped during suspend modes.
SUSCLK	O	**SUSPEND CLOCK.** 32.768-kHz output clock provided to the Host-to-PCI bridge used for maintenance of DRAM refresh. This signal is stopped during Suspend-to-Disk and Soft Off modes. For values During Reset, After Reset, and During POS, see the *Suspend/Resume and Resume Control Signaling* section.
SYSCLK	O	**ISA SYSTEM CLOCK.** SYSCLK is the reference clock for the ISA bus. It drives the ISA bus directly. The SYSCLK is generated by dividing PCICLK by 4. The SYSCLK frequencies supported are 7.5 MHz and 8.33 MHz. For PCI accesses to the ISA bus, SYSCLK may be stretched low to synchronize BALE falling to the rising edge of SYSCLK. **During Reset:** Running **After Reset:** Running **During POS:** Low
PDA[2:0]	O	**PRIMARY DISK ADDRESS[2:0].** These signals indicate which byte in either the ATA command block or control block is being addressed. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Primary IDE connector. If the IDE signals are configured for Primary 0 and Primary 1, these signals are used for the Primary 0 connector.
PDCS1#	O	**PRIMARY DISK CHIP SELECT FOR 1F0H– –1F7H RANGE.** For ATA command register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. **During Reset:** High **After Reset:** High **During POS:** High
PDCS3#	O	**PRIMARY DISK CHIP SELECT FOR 3F0– –3F7 RANGE.** For ATA control register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. **During Reset:** High **After Reset:** High **During POS:** High
PDD[15:0]	I/O	**PRIMARY DISK DATA[15:0].** These signals are used to transfer data to or from the IDE device. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector.
SDA[2:0]	O	**SECONDARY DISK ADDRESS[2:0].** These signals indicate which byte in either the ATA command block or control block is being addressed. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector.

5.2 INTEL 82371EB PCI-TO-ISA / IDE XCELERATOR (PIIX4) (6).

SIGNAL	TYPE	DESCRIPTION
PDDACK#	O	**PRIMARY DMA ACKNOWLEDGE.** This signal directly drives the IDE device DMACK# signal. It is asserted by PIIX4 to indicate to IDE DMA slave devices that a given data transfer cycle (assertion of PDIOR# or PDIOW#) is a DMA data transfer cycle. This signal is used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. **During Reset:** High **After Reset:** High **During POS:** High
PDDREQ	I	**PRIMARY DISK DMA REQUEST.** This input signal is directly driven from the IDE device DMARQ signal. It is asserted by the IDE device to request a data transfer, and used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector.
PDIOR#	O	**PRIMARY DISK IO READ.** In normal IDE this is the command to the IDE device that it may drive data onto the PDD[15:0] lines. Data is latched by PIIX4 on the negation edge of PDIOR#. The IDE device is selected either by the ATA register file chip selects (PDCS1#, PDCS3#) and the PDA[2:0] lines, or the IDE DMA slave arbitration signals (PDDACK#). In an Ultra DMA/33 read cycle, this signal is used as DMARDY# which is negated by the PIIX4 to pause Ultra DMA/33 transfers. In an Ultra DMA/33 write cycle, this signal is used as the STROBE signal, with the drive latching data on rising and falling edges of STROBE. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector.
PDIOW#	O	**PRIMARY DISK IO WRITE.** In normal IDE mode, this is the command to the IDE device that it may latch data from the PDD[15:0] lines. Data is latched by the IDE device on the negation edge of PDIOW#. The IDE device is selected either by the ATA register file chip selects (PDCS1#, PDCS3#) and the PDA[2:0] lines, or the IDE DMA slave arbitration signals (PDDACK#). For Ultra DMA/33 mode, this signal is used as the STOP signal, which is used to terminate an Ultra DMA/33 transaction. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector.
PIORDY	I	**PRIMARY IO CHANNEL READY.** In normal IDE mode, this input signal is directly driven by the corresponding IDE device IORDY signal. In an Ultra DMA/33 read cycle, this signal is used as STROBE, with the PIIX4 latching data on rising and falling edges of STROBE. In an Ultra DMA/33 write cycle, this signal is used as the DMARDY# signal which is negated by the drive to pause Ultra DMA/33 transfers.

SIGNAL	TYPE	DESCRIPTION
SDCS1#	O	**SECONDARY CHIP SELECT FOR 170H– –177H RANGE.** For ATA command register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. **During Reset:** High **After Reset:** High **During POS:** High
SDCS3#	O	**SECONDARY CHIP SELECT FOR 370H– –377H RANGE.** For ATA control register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. **During Reset:** High **After Reset:** High **During POS:** High-Z
SDD[15:0]	I/O	**SECONDARY DISK DATA[15:0].** These signals are used to transfer data to or from the IDE device. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector.
SDDACK#	O	**SECONDARY DMA ACKNOWLEDGE.** This signal directly drives the IDE device DMACK# signal. It is asserted by PIIX4 to indicate to IDE DMA slave devices that a given data transfer cycle (assertion of SDIOR# or SDIOW#) is a DMA data transfer cycle. This signal is used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. **During Reset:** High **After Reset:** High **During POS:** High
SDDREQ	I	**SECONDARY DISK DMA REQUEST.** This input signal is directly driven from the IDE device DMARQ signal. It is asserted by the IDE device to request a data transfer, and used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector.
SDIOR#	O	**SECONDARY DISK IO READ.** In normal IDE mode, this is the command to the IDE device that it may drive data onto the SDD[15:0] lines. Data is latched by the PIIX4 on the negation edge of SDIOR#. The IDE device is selected either by the ATA register file chip selects (SDCS1#, SDCS3#) and the SDA[2:0] lines, or the IDE DMA slave arbitration signals (SDDACK#). In an Ultra DMA/33 read cycle, this signal is used as DMARDY# which is negated by the PIIX4 to pause Ultra DMA/33 transfers. In an Ultra DMA/33 write cycle, this signal is used as the STROBE signal, with the drive latching data on rising and falling edges of STROBE. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector.

5.2 INTEL 82371EB PCI-TO-ISA / IDE XCELERATOR (PIIX4) (7).

SIGNAL	TYPE	DESCRIPTION
SDIOW#	O	**SECONDARY DISK IO WRITE.** In normal IDE mode, this is the command to the IDE device that it may latch data from the SDD[15:0] lines. Data is latched by the IDE device on the negation edge of SDIOW#. The IDE device is selected either by the ATA register file chip selects (SDCS1#, SDCS3#) and the SDA[2:0] lines, or the IDE DMA slave arbitration signals (SDDACK#). In read and write cycles this signal is used as the STOP signal, which is used to terminate an Ultra DMA/33 transaction. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. **During Reset:** High **After Reset:** High **During POS:** High
SIORDY	I	**SECONDARY IO CHANNEL READY.** In normal IDE mode, this input signal is directly driven by the corresponding IDE device IORDY signal. In an Ultra DMA/33 read cycle, this signal is used as STROBE, with the PIIX4 latching data on rising and falling edges of STROBE. In an Ultra DMA write cycle, this signal is used as the DMARDY# signal which is negated by the drive to pause Ultra DMA/33 transfers. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. This is a Schmitt triggered input.
OC[1:0]#	I	**OVER CURRENT DETECT.** These signals are used to monitor the status of the USB power supply lines. The corresponding USB port is disabled when its over current signal is asserted.
USBP0+, USBP0□	I/O	**SERIAL BUS PORT 0.** This signal pair comprises the differential data signal for USB port 0.
USBP1+, USBP1	I/O	**SERIAL BUS PORT 1.** This signal pair comprises the differential data signal for USB port 1.
BATLOW#/ GPI9	I	**BATTERY LOW.** Indicates that battery power is low. PIIX4 can be programmed to prevent a resume operation when the BATLOW# signal is asserted. If the Battery Low function is not needed, this pin can be used as a general-purpose input.
CPU_STP#/ GPO17	O	**CPU CLOCK STOP.** Active low control signal to the clock generator used to disable the CPU clock outputs. If this function is not needed, then this signal can be used as a general-purpose output. For values **During Reset**, **After Reset**, and **During POS**, see the *Suspend/Resume and Resume Control Signaling* section.
EXTSMI#	I/OD	**EXTERNAL SYSTEM MANAGEMENT INTERRUPT.** EXTSMI# is a falling edge triggered input to PIIX4 indicating that an external device is requesting the system to enter SMM mode. When enabled, a falling edge on EXTSMI# results in the assertion of the SMI# signal to the CPU. EXTSMI# is an asynchronous input to PIIX4. However, when the setup and hold times are met, it is only required to be asserted for one PCICLK. Once negated EXTSMI# must remain negated for at least four PCICLKs to allow the edge detect logic to reset. EXTSMI# is asserted by PIIX4 in response to SMI# being activated within the Serial IRQ function. An external pull-up should be placed on this signal.

SIGNAL	TYPE	DESCRIPTION
LID/ GPI10	I	**LID INPUT.** This signal can be used to monitor the opening and closing of the display lid of a notebook computer. It can be used to detect both low to high transition or a high to low transition and these transitions will generate an SMI# if enabled. This input contains logic to perform a 16-ms debounce of the input signal. If the LID function is not needed, this pin can be used as a general-purpose input.
PCIREQ[A:D]#	I	**PCI REQUEST.** Power Management input signals used to monitor PCI Master Requests for use of the PCI bus. They are connected to the corresponding REQ[0:3]# signals on the Host Bridge.
PCI_STP#/ GPO18	O	**PCI CLOCK STOP.** Active low control signal to the clock generator used to disable the PCI clock outputs. The PIIX4 free running PCICLK input must remain on. If this function is not needed, this pin can be used as a general-purpose output. For values **During Reset**, **After Reset**, and **During POS**, see the *Suspend/Resume and Resume Control Signaling* section.
PWRBTN#	I	**POWER BUTTON.** Input used by power management logic to monitor external system events, most typically a system on/off button or switch. This input contains logic to perform a 16-ms debounce of the input signal.
RI# GPI12	I	**RING INDICATE.** Input used by power management logic to monitor external system events, most typically used for wake up from a modem. If this function is not needed, then this signal can be individually used as a general-purpose input.
RSMRST#	I	**RESUME RESET.** This signal resets the internal Suspend Well power plane logic and portions of the RTC well logic.
SMBALERT#/ GPI11	I	**SM BUS ALERT.** Input used by System Management Bus logic to generate an interrupt (IRQ or SMI) or power management resume event when enabled. If this function is not needed, this pin can be used as a general-purpose input.
SMBCLK	I/O	**SM BUS CLOCK.** System Management Bus Clock used to synchronize transfer of data on SMBus. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
SMBDATA	I/O	**SM BUS DATA.** Serial data line used to transfer data on SMBus. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
SUSA#	O	**SUSPEND PLANE A CONTROL.** Control signal asserted during power management suspend states. SUSA# is primarily used to control the primary power plane. This signal is asserted during POS, STR, and STD suspend states. **During Reset:** Low **After Reset:** High **During POS:** Low
SUSB#/ GPO15	O	**SUSPEND PLANE B CONTROL.** Control signal asserted during power management suspend states. SUSB# is primarily used to control the secondary power plane. This signal is asserted during STR and STD suspend states. If the power plane control is not needed, this pin can be used as a general-purpose output. **During Reset:** Low **After Reset:** High **During POS:** High/GPO
SUSC#/ GPO16	O	**SUSPEND PLANE C CONTROL.** Control signal asserted during power management suspend states, primarily used to control the tertiary power plane. It is asserted only during STD suspend state. If the power plane control is not needed, this pin can be used as a general-purpose output. **During Reset:** Low **After Reset:** High **During POS:** High/GPO
SUS_STAT1#/ GPO20	O	**SUSPEND STATUS 1.** This signal is typically connected to the Host-to-PCI bridge and is used to provide information on host clock status. SUS_STAST1# is asserted when the system may stop the host clock, such as Stop Clock or during POS, STR, and STD suspend states. If this function is not needed, this pin can be used as a general-purpose output.

5.2 INTEL 82371EB PCI-TO-ISA / IDE XCELERATOR (PIIX4) (8).

SIGNAL	TYPE	DESCRIPTION
SUS_STAT2#/ GPO21	O	**SUSPEND STATUS 2.** This signal will typically connect to other system peripherals and is used to provide information on system suspend state. It is asserted during POS, STR, and STD suspend states. If this function is not needed, this pin can be used as a general-purpose output. **During Reset:** Low **After Reset:** High **During POS:** Low/GPO
THRM#/ GPI8	I	**THERMAL DETECT.** Active low signal generated by external hardware to start the Hardware Clock Throttling mode. If enabled, the external hardware can force the system to enter into Hardware Clock Throttle mode by asserting THRM#. This causes PIIX4 to cycle STPCLK# at a preset programmable rate. If this function is not needed, this pin can be used as a general-purpose input.
ZZ/ GPO19	O	**LOW-POWER MODE FOR L2 CACHE SRAM.** This signal is used to power down a cache□ data SRAMs when the clock logic places the CPU into the Stop Clock. If this function is not needed, this pin can be used as a general-purpose output. **During Reset:** Low **After Reset:** Low **During POS:** Low
GPI[21:0]	I	**GENERAL PURPOSE INPUTS.** These input signals can be monitored via the GPIREG register located in Function 3 (Power Management) System IO Space at address PMBase+30h. See Table 1 for details.
GPO[30:0]	O	**GENERAL PURPOSE OUTPUTS.** These output signals can be controlled via the GPIREG register located in Function 3 (Power Management) System IO Space at address PMBase+34h. If a GPO pin is not multiplexed with another signal or defaults to GPO, then its state after reset is the reset condition of the GPOREG register. If the GPO defaults to another signal, then it defaults to that signal□ state after reset. The GPO pins that default to GPO remain stable after reset. The others may toggle due to system boot or power control sequencing after reset prior to their being programmed as GPOs. The GPO8 signal is driven low upon removal of power from the PIIX4 core power plane. All other GPO signals are invalid (buffers powered off).
CONFIG1	I	**CONFIGURATION SELECT 1.** This input signal is used to select the type of microprocessor being used in the system. If CONFIG1=0, the system contains a Pentium microprocessor. If CONFIG1=1, the system contains a Pentium II microprocessor. It is used to control the polarity of INIT and CPURST signals.
CONFIG2	I	**CONFIGURATION SELECT 2.** This input signal is used to select the positive or subtractive decode of FFFF0000h□FFFFFFFh memory address range (top 64 Kbytes). If CONFIG[2]=0, the PIIX4 will positively decode this range. If CONFIG[2]=1, the PIIX4 will decode this range with subtractive decode timings only. The input value of this pin must be static and may not dynamically change during system operations.
PWROK	I	**POWER OK.** When asserted, PWROK is an indication to PIIX4 that power and PCICLK have been stable for at least 1 ms. PWROK can be driven asynchronously. When PWROK is negated, PIIX4 asserts CPURST, PCIRST# and RSTDRV. When PWROK is driven active (high), PIIX4 negates CPURST, PCIRST#, and RSTDRV.
SPKR	O	**SPEAKER.** The SPKR signal is the output of counter timer 2 and is internally "ANDed" with Port 061h bit 1 to provide the Speaker Data Enable. This signal drives an external speaker driver device, which in turn drives the ISA system speaker. **During Reset:** Low **After Reset:** Low **During POS:** Last State TEST# I **TEST MODE SELECT.** The test signal is used to select various test modes of PIIX4. This signal must be pulled up to VCC(SUS) for normal operation.

SIGNAL	TYPE	DESCRIPTION
VCC	V	**CORE VOLTAGE SUPPLY.** These pins are the primary voltage supply for the PIIX4 core and IO periphery and must be tied to 3.3V.
VCC (RTC)	V	**RTC WELL VOLTAGE SUPPLY.** This pin is the supply voltage for the RTC logic and must be tied to 3.3V.
VCC (SUS)	V	**SUSPEND WELL VOLTAGE SUPPLY.** These pins are the primary voltage supply for the PIIX4 suspend logic and IO signals and must be tied to 3.3V.
VCC (USB)	V	**USB VOLTAGE SUPPLY.** This pin is the supply voltage for the USB input/output buffers and must be tied to 3.3V.
VREF	V	**VOLTAGE REFERENCE.** This pin is used to provide a 5V reference voltage for 5V safe input buffers. VREF must be tied to 5V in a system requiring 5V tolerance. In a 5V tolerant system, this signal must power up before or simultaneous to VCC. It must power down after or simultaneous to VCC. In a non-5V tolerant system (3.3V only), this signal can be tied directly to VCC. There are then no sequencing requirements.
VSS	V	**CORE GROUND.** These pins are the primary ground for PIIX4.
VSS (USB)	V	**USB GROUND.** This pin is the ground for the USB input/output buffers.

6. MAJOR CHIP DESCRIPTION

6.1 SYSTEM CONTROLLER: INTEL 82439TX (MTXC)

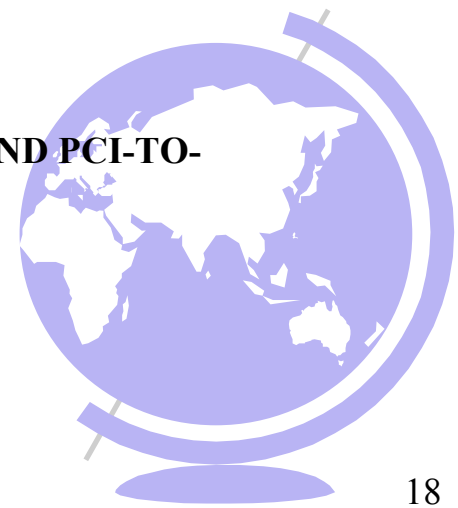
- HOST BRIDGE (NORTH BRIDGE) FOR TRANSLATION FROM CPU BUS CYCLE TO PCI BUS CYCLE

- DRAM MEMORY CONTROLLER
  - ~ 64-BIT DATA WIDTH
  - ~ SUPPORTS FPM, EDO, SDRAM
  - ~ SUPPORTS 64M BIT EDO (MA[0…11]) AND SYNCHRONOUS (MA[0…13]) DRAM ORGANIZATION
  - ~ MIXING INSTALLATION OF ANY TYPE OF DRAM
  - ~ AUTO DETECTION OF DRAM TYPE

- LEVEL 2 CACHE CONTROLLER
  - ~ DIRECT MAPPED WITH WRITE-BACK ALGORITHM
  - ~ SUPPORT BOTH 256K AND 512K CONFIGURATION

- TWO UNIVER DATAPATH AND BUFFERS
  - ~ 5 QWORD BUFFER FOR CPU TO DRAM, L2 CACHE WRITE-BACK AND PCI-TO-DRAM TRANSFERS
  - ~ 5 QWORD BUFFER FOR CPU-TO-PCI WRITES
  - ~ 5 QWORD PREFETCHING BUFFER FOR PCI-TO-DRAM READ PATH
  - ~ 18 D WORD BUFFER FOR PCI-TO-DRAM WRITES

- BUS ARBITER
  - ~ SUPPORTS 5 PCI BUS MASTERS (4 GENERAL BUS MASTER + PIIX4)



6.2 INTEL 82371EB PCI-TO-ISA / IDE XCELERATOR (PIIX4E)

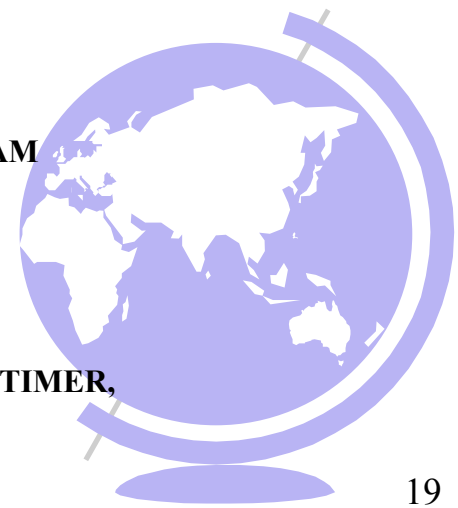
- MULTI FUNCTION PCI DEVICES
  - ~ PCI-TO-ISA/EIO BRIDGE FOR PASSING THE CYCLES ACCESSING ISA
  - ~ PCI IDE WITH ULTRA DMA/33 SUPPORT
  - ~ UNIVERSAL SERIAL BUS PORT
  - ~ ENHANCED POWER MANAGEMENT
  - ~ COMMON I/O FUNCTIONS

- PCI IDE CONTROLLER
  - ~ SUPPORT 2 CHANNELS WITH 4 DEVICES
  - ~ PIO MODE 4 TRANSFERS UP TO 14MBPS
  - ~ SUPPORTS BUS MASTER IDE
  - ~ ULTRA DMA/33 TRANSFERS UP TO 33MBS
  - ~ 8 * 32 BIT BUFFER FOR PCI IDE BURST TRNASFERS

- USB
  - ~ SUPPORTS LEGACY KEYBOARD AND MOUSE
  - ~ UNIVERSAL HOST CONTROLLER INTERFACE (UHCI) REVISION 1.1 INTERFACE

- ENHANCED POWER MANAGEMENT
  - ~ GLOBAL AND LOCAL DEVICE (14 DEVICES) MANAGEMENT & SUPPORT ACPI
  - ~ FULL CLOCK CONTROL: CLOCK THROTTLING, STOP CLOCK
  - ~ DIFFERENT DEPTH OF SUSPEND: POWER ON SUSPEND (POS), SUSPEND TO DRAM (STR), SUSPEND TO DISK (STD)
  - ~ SYSTEM MANAGEMENT MODE (SMM) SUPPORT

- ISA/EIO INTERFACE AND COMMON I/O DEVICES
  - ~ CAN BE CONFIGURED AS FULL ISA OR SUBSET OF FULL ISA (EXTENDED I/O)
  - ~ TWO 8237 DMA CONTROLLER, TWO 8259 INTERRUPT CONTROLLER, ONE 8254 TIMER, ONE MC146818A COMPATIBLE REAL-TIME CLOCK (RTC)



7. SYSTEM VIEW AND DISASSEMBLY

7.1 System View

7.1.1 Right-Side view

1. **CD-ROM Drive**
2. **IR Port**

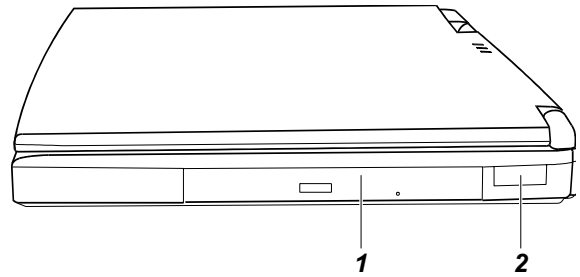


Figure 7-1. Right-Side View

7.1.2 Left-Side View

1. **Phone Line Connector** (optional)
2. **Kensington Lock Anchor**
3. **PC Card Slots**
4. **Floppy Disk Drive**

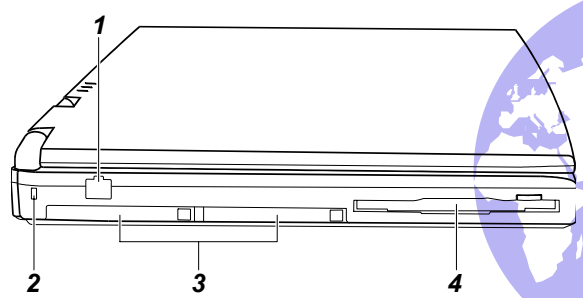


Figure 7-2. Left-Side View

7.1 System View

7.1.3 Rear View

1. **Power Connector**
2. **PS/2 Mouse/Keyboard Port**
3. **USB Port**
4. **Expansion Connector**
5. **Serial Port**
6. **S-Video Output Connector**
7. **Parallel Port**
8. **VGA Port**

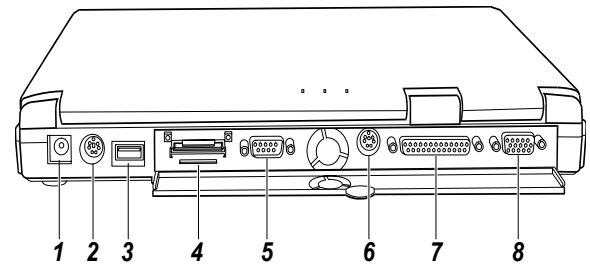


Figure 7-3. Rear View

7.1.4 Front View

1. **Top Cover Latch**
2. **Microphone Connector**
3. **Audio Output Connector**

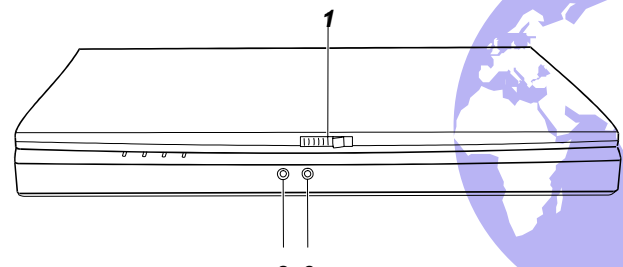


Figure 7-4. Front View

7.1 System View

7.1.5 Bottom View

1. **Battery Pack**
2. **Ventilation Openings**
3. **SO-DIMM Compartment Cover**
4. **CMOS Battery Compartment Cover**

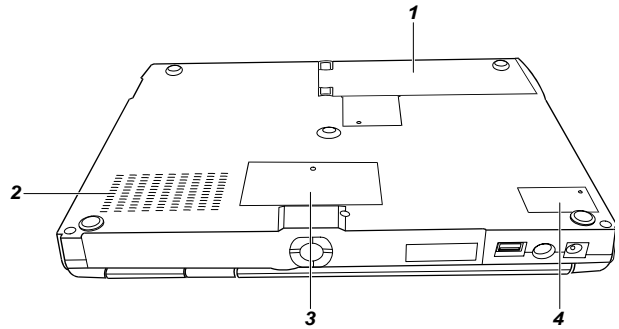


Figure 7-5. Bottom View

7.1.6 Top-Open View

To open the cover, press the cover latch toward the right and lift the cover.

1. **Microphone**
2. **LCD Display**
3. **Suspend Button**
4. **Stereo Speaker Set**
5. **Keyboard**
6. **Device Indicators**
7. **Touchpad**
8. **Power Button**
9. **System Indicators**

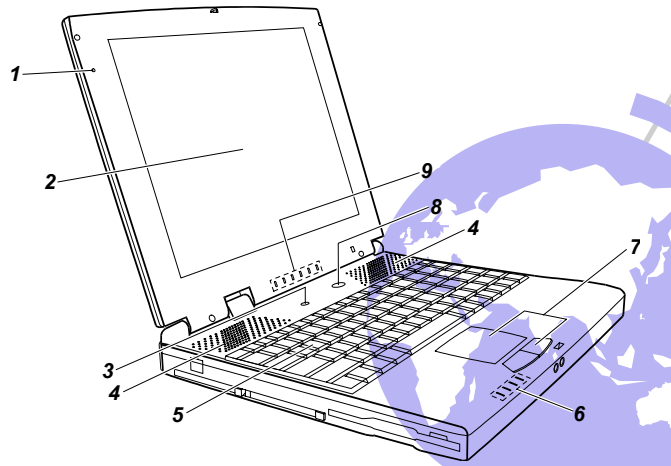


Figure 7-6. Top-Open View

7.2 System Disassembly

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations. Use the chart below to determine the disassembly sequence for removing components from the notebook.

Modular Components

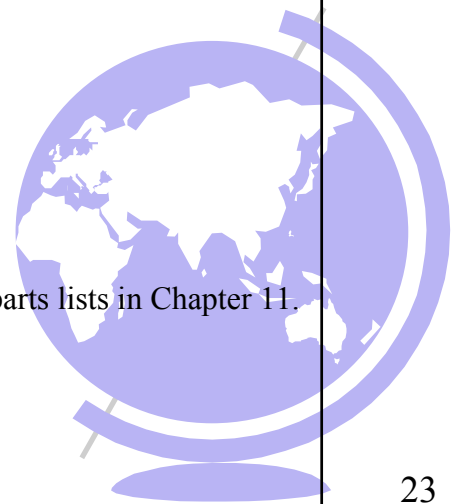
- 7.2.1 Battery Pack
- 7.2.2 CD-ROM Drive
- 7.2.3 SO-DIMM
- 7.2.4 CMOS Battery

LCD Assembly Components

- 7.2.5 LCD Assembly
- 7.2.6 LCD Panel
- 7.2.7 Inverter Board/LED Board

Base Unit Components

- 7.2.8 Keyboard
- 7.2.9 CPU BOARD
- 7.2.10 Fax/Modem/Voice Card
- 7.2.11 Hard Disk Drive
- 7.2.12 Touchpad Board
- 7.2.13 System Board
- 7.2.14 Floppy Disk Drive



You can also find details such as exploded views and parts lists in Chapter 11.

7.2 System Disassembly

7.2.1 Battery Pack

- Disassembly

1. Place the notebook upside down.
2. First push away the locking latches and then lift the battery pack out of the compartment.

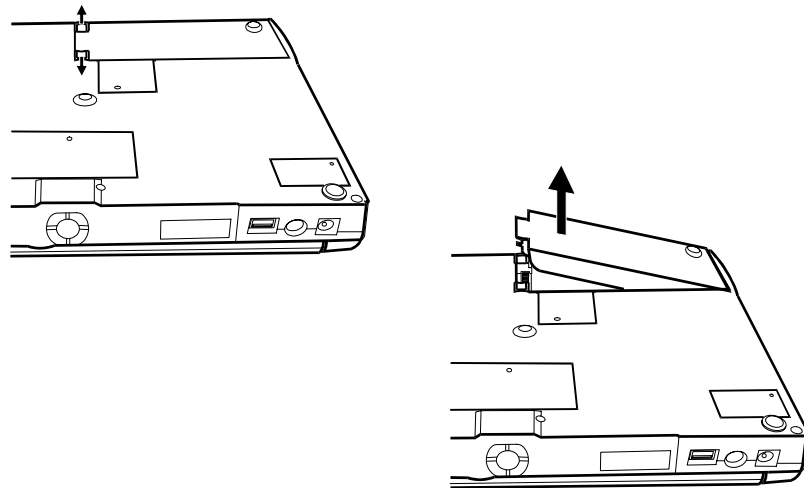


Figure 7-7. Removing the Battery Pack

- Reassembly

. Fit the battery pack into the compartment. Make sure the locking latches are in the locked position. (Refer to Figure 7-7 earlier.)

7.2 System Disassembly

7 .2.2 CD-ROM Drive

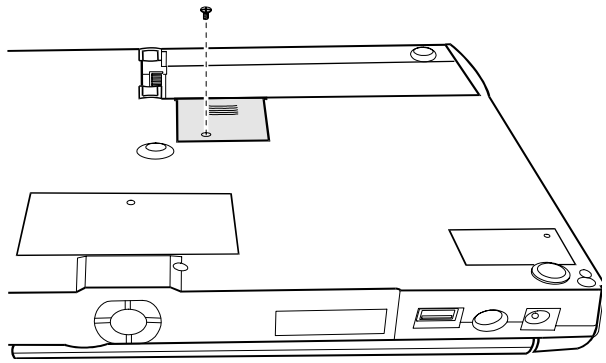


Figure 7-8. Removing the CD-ROM Drive Connector Cover

- Disassembly

1. Place the notebook upside down.
2. Remove the battery pack. (Refer to Figure 7-7 earlier.)
3. Remove the CD-ROM drive connector cover by removing one screw and pushing the cover outward.
4. Unplug the cable from the system board
5. Remove the CD-ROM drive by sliding it out of the compartment.

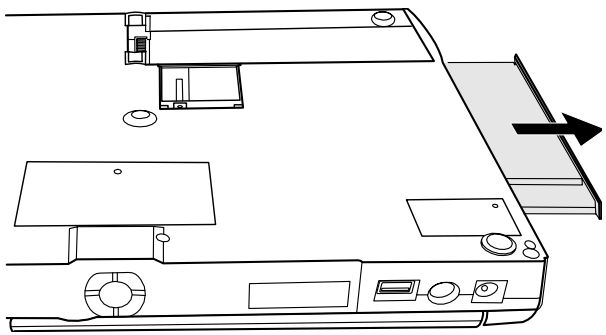


Figure 7-10. Removing the CD-ROM Drive

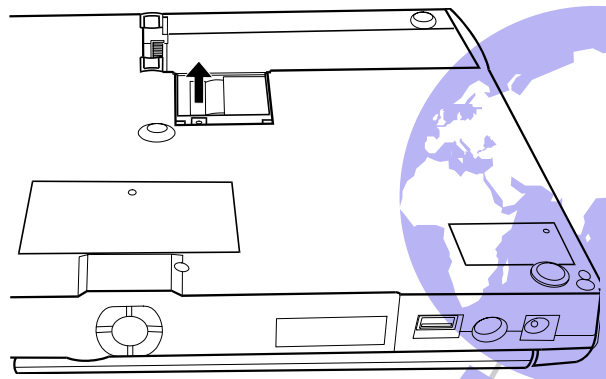


Figure 7-9. Unplugging the CD-ROM Drive Cable

7.2 System Disassembly

●Reassembly

1. Remove the battery pack. (Refer to Figure 7-7 earlier.)
2. Remove the CD-ROM drive connector cover.
   (Refer to Figure 7-8 earlier.)
3. Connect one end of the CD-ROM drive cable to the CD-ROM drive.
4 Slide the CD-ROM drive into the compartment.
   (Refer to Figure 7-10 earlier.)
5. Connect the CD-ROM drive cable to the system board.
   (Refer to Figure 7-9 earlier.)
6. Replace the CD-ROM drive connector cover and secure the cover with one screw. (Refer to Figure 7-8 earlier.)

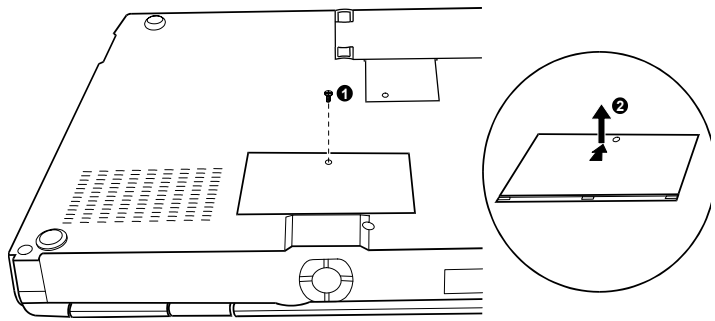


Figure 7-11. Removing the SO-DIMM Compartment Cover

7.2.3 SO-DIMM

●Disassembly

1. Remove one screw and push upward to open the compartment cover.
2. Pull the retaining clips outwards and remove the SO-DIMM.

7.2 System Disassembly

●Reassembly

1. To install the SO-DIMM, align the SO-DIMM′ s notched end with the socket′ s corresponding end and firmly insert the SO-DIMM into the socket at an angle. Then push down until the retaining clips lock the SO-DIMM into position. (Refer to Figure 7-12)
2. Replace the compartment cover and secure with one screw. (Refer to Figure 7-11 earlier.)

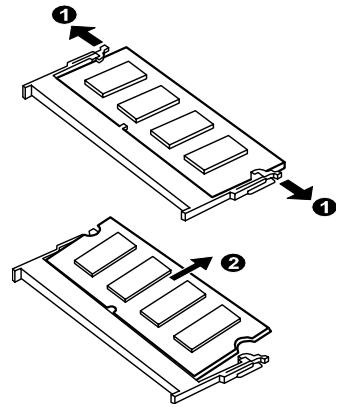


Figure 7-12. Removing the SO-DIMM

7.2.4 CMOS Battery

●Disassembly

1. Put the notebook upside down with care.
2. To access the CMOS battery, remove one screw and slide the compartment cover toward the left to open the cover.
3. Remove the battery by inserting a flat screw driver to push it out of the battery holder.

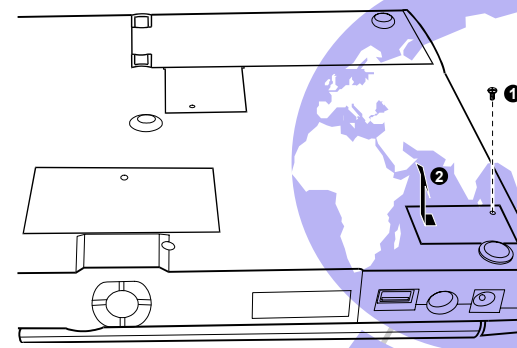


Figure 7-13. Removing the CMOS Battery Cover

7.2 System Disassembly

•Reassembly

1. Fit the CMOS battery into place. (Refer to Figure 7-14)
2. Replace the battery cover and secure with one screw. (Refer to Figure 7-13 earlier.)

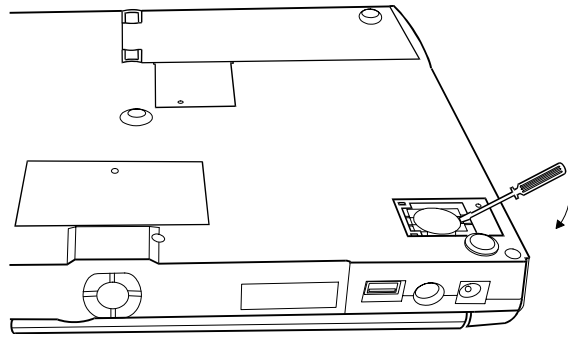


Figure 7-14. Removing the CMOS Battery

7.2.5 LCD Assembly

1. Open the top cover and remove the two hinge covers.
2. Slightly move the speaker panel downward and lift it up.
3. Remove the four screws fastening the LCD display with the hinges. Then remove the wire cover and unplug the LCD cable connecting to the system board. Now you can separate the LCD assembly from the base unit.

•Reassembly

1. Replace four screws, reconnect the LCD cable connectors to the system board and replace the wire cover. (Refer to Figure7-17)

7.2 System Disassembly

2. Replace the speaker panel. (Refer to Figure7-16)
3. Replace the hinge covers. (Refer to Figure7-15)

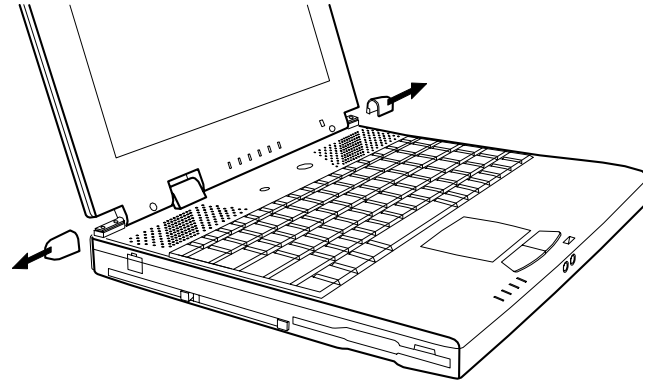


Figure 7-15. Removing the Hinge Covers

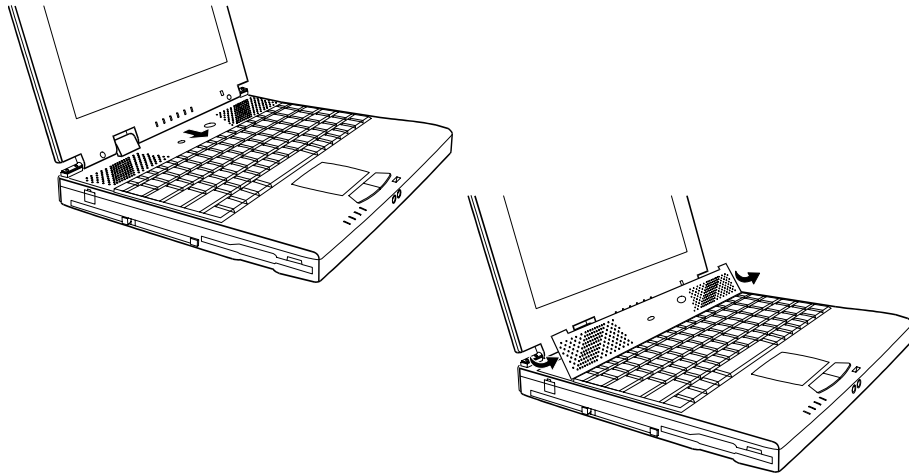


Figure 7-16. Removing the Speaker Panel

7.2 System Disassembly

2.2.6 LCD Panel

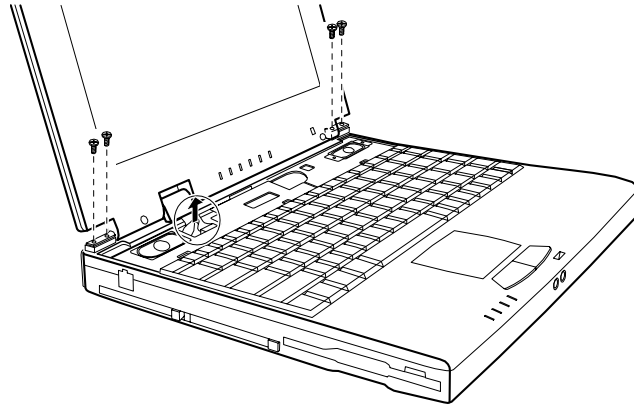


Figure 7-17. Removing the Screws and Unplugging the LCD Cable Connectors

●Disassembly

1. Open the top cover.
2. Remove the four screws on the LCD panel. Now you can separate the LCD frame from the housing.
3. To remove the LCD, remove four screws and unplug the cables.

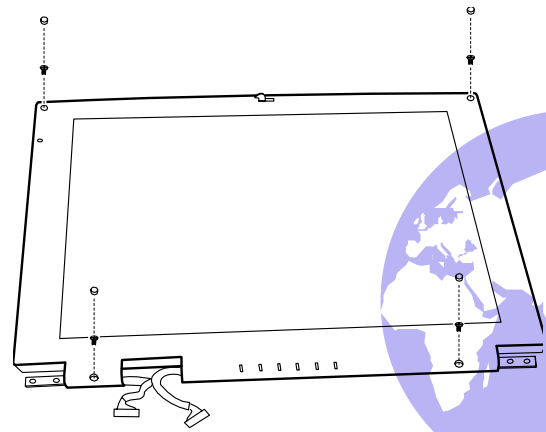


Figure 7-18. Removing the LCD Frame

●Reassembly

1. Reconnect the cables to the LCD. Fit the LCD back into place and secure with four screws. (Refer to Figure 7-19)
2. Fit the LCD frame back to the housing and secure with four screws. (Refer to Figure 7-18)

7.2 System Disassembly

7.2.7 LED Board

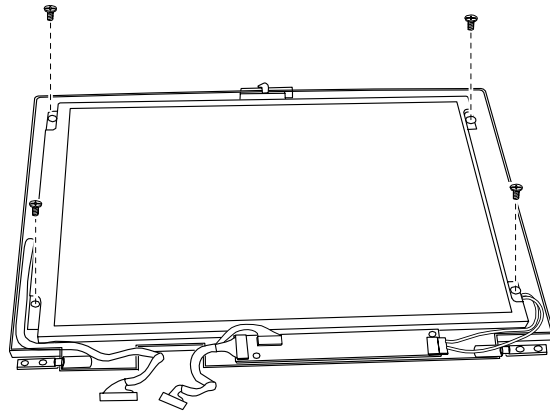


Figure7-19. Removing the Flat Panel Screen

●Disassembly

1. Detach the LCD frame. (See section 7.2.6 Disassembly.)
2. To remove the LED board at the bottom side of the LCD , remove two screws and unplug the connectors from the board.

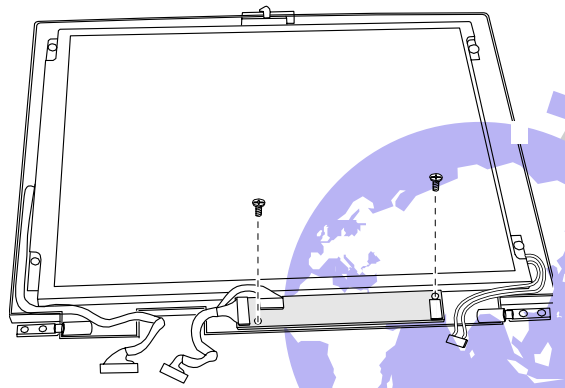


Figure 7-20. Removing the LED Board

●Reassembly

1. Reconnect the connectors. Fit the LED board back into place and secure with two screws. (Refer to Figure7-20)
2. Fit the LCD frame back to the housing and replace the four screws. (See section 7.2.6 Reassembly step 2.)

7.2 System Disassembly

7.2.8 Keyboard

●Disassembly

1. Open the top cover. Remove the two hinge covers and the speaker panel. (See section 7.2.5 Disassembly step 1 to 2.)
2. Remove three screws fastening the keyboard.

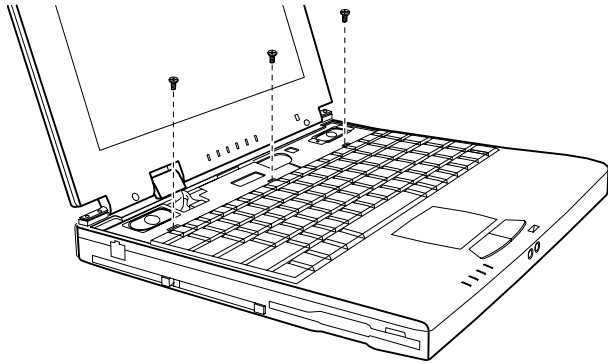


Figure 7-21. Removing Three Screws

●Reassembly

1. Reconnect the keyboard cable and fit the keyboard back into place. (Refer to Figure 7-22)
2. Replace three screws. (Refer to Figure 7-21 earlier.)
3. Replace the speaker panel and the two hinge covers. (See section 7.2.5 Reassembly step 2 to 3.)

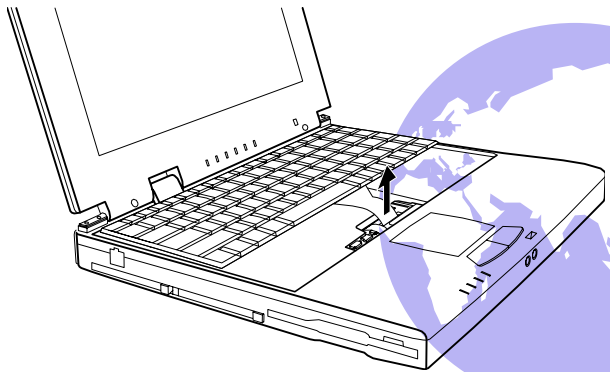


Figure 7-22. Disconnecting the Keyboard Cable

7.2 System Disassembly

7.2.9 CPU BOARD

●Disassembly

1. Open the top cover. Remove the two hinge covers and the speaker panel. (See section 7.2.5 Disassembly step 1 to 2.)
2. Remove the keyboard. (See section 7.2.8 Disassembly step 2 to 3.)
3. Remove four screws from the metal plate.
   Slide the plate toward the right, then toward the speaker, and finally lift it up.
4. To remove the CPU board, slightly lift the CPU board out of the three screw nuts on the system board and unplug the connector.

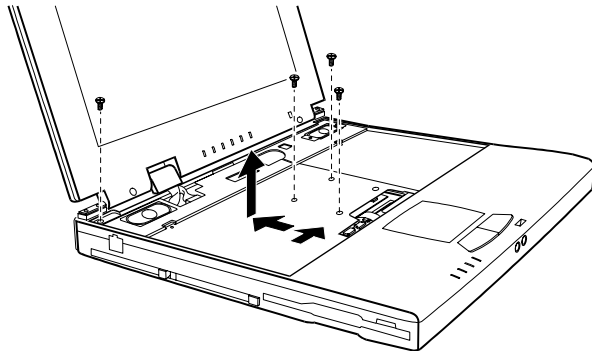


Figure 7-23. Removing the Metal Plate

●Reassembly

1. Align the three holes on the CPU board with the three screw nuts on the system Board and plug the CPU board connector into the corresponding connector. (Refer to Figure 7-24)
2. Replace the metal plate and secure with four screws. (Refer to Figure 7-23)
3. Replace the keyboard and secure with three screws. (See section 7.2.8 Reassembly step 1 to 2.)

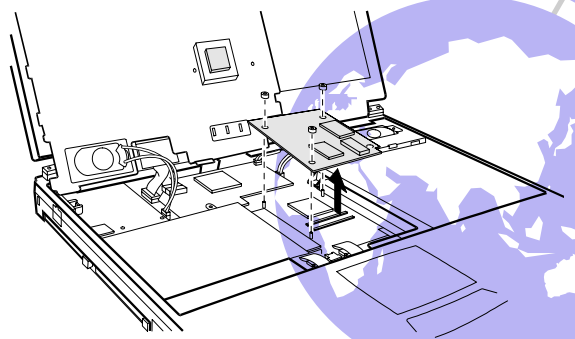


Figure 7-24. Removing the CPU Card

7.2 System Disassembly

4. Replace the speaker panel and the two hinge covers.
   (See section 7.2.5 Reassembly step 2 to 3.)

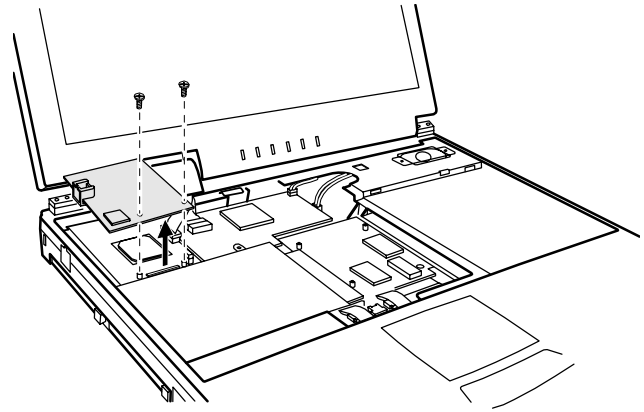


Figure 7-25. Removing the Fax/Modem/Voice Card

7.2.10 Fax/Modem/Voice Card

•Disassembly

1. Open the top cover. Remove the two hinge covers and the speaker panel.
   (See section 7.2.5 Disassembly step 1 to 2.)
2. Remove the keyboard. (See section 7.2.8 Disassembly step 2 to 3.)
3. Remove the metal plate. (See section 7.2.9 Disassembly step 3.)
4. Remove two screws and lift up the Fax/Modem/Voice Card to disconnect the connector from the system board

7.2 System Disassembly

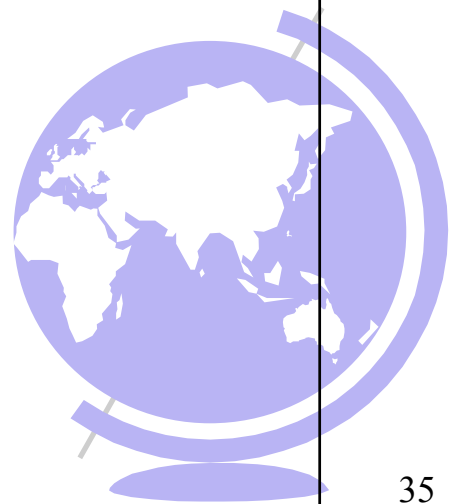
•Reassembly

1. Hold the Fax/Modem/Voice Card at an angle so that the phone line connector is pointed towards the opening on the notebook. Insert the phone line connector into the opening and press the other end to plug the other connector into the socket on the system board. Then, secure with two screws. (Refer to Figure 7-25 earlier.)
2. Replace the metal plate and secure with four screws. (See section 7.2.9 Reassembly step 2.)
3. Replace the keyboard and secure with three screws. (See section 7.2.8 Reassembly step 1 to 2.)
4. Replace the speaker panel and the two hinge covers. (See section 7.2.5 Reassembly step 2 to 3.)

7.2.11 Hard Disk Drive

•Disassembly

1. Open the top cover. Remove the two hinge covers and the speaker panel. (See section 7.2.5 Disassembly step 1 to 2.)
2. Remove the keyboard. (See section 7.2.8 Disassembly step 2 to 3.)
3. Remove the metal plate. (See section 7.2.9 Disassembly step 3.)
4. Remove two screws fastening the hard disk drive bracket and unplug the cable connector.



7.2 System Disassembly

5. To separate the hard disk drive from the bracket, remove four side screws from the bracket.

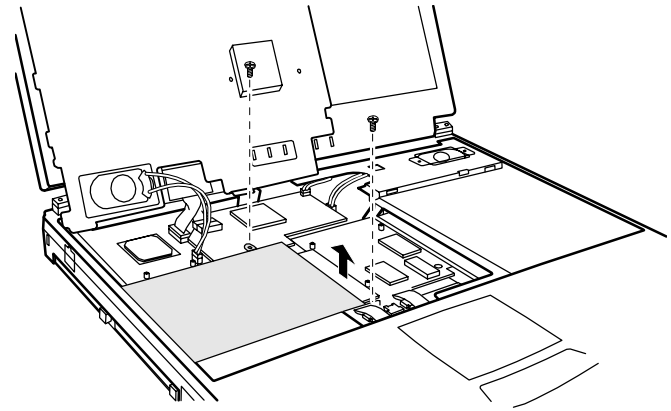


Figure 7-26. Removing the Hard Disk Drive

•Reassembly

1. Attach the bracket to the hard disk drive and secure with four screws on both sides. (Refer to Figure 7-27)
2. Plug the hard disk drive connector to the system board and secure the bracket in place with two screws. (Refer to Figure 7-26)
3. Replace the metal plate and secure with four screws. (See section 7.2.9 Reassembly step 2.)
4. Replace the keyboard and secure with three screws. (See section 7.2.8 Reassembly step 1 to 2.)
5. Replace the speaker panel and the two hinge covers. (See section 7.2.5 Reassembly step 2 to 3.)

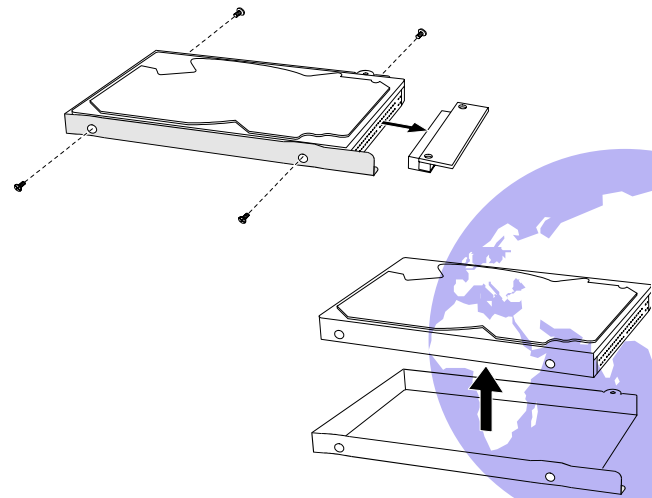


Figure 7-27. Removing the Hard Disk Drive Bracket

7.2 System Disassembly

7.2.12 Touchpad Board

●Disassembly

1. Open the top cover. Remove the two hinge covers and the speaker panel. (See section 7.2.5 Disassembly step 1 to 2.)
2. Remove the keyboard. (See section 7.2.8 Disassembly step 2 to 3.)
3. Remove the metal plate. (See section 7.2.9 Disassembly step 3.)
4. Remove the LCD display. (See section 7.2.5 Disassembly.)
5. Place the notebook upside down with care.
6. Remove the battery pack. (See section7.2.1 Disassembly step 2.)
7. Remove eight screws on the bottom and three screws on the rear side which fix the surface frame with the bottom base.
8. Place the notebook surface up. Unplug two speaker connectors and two touchpad cables connecting to the Audio/Charger board. Remove two screws fastening the surface frame with the system board.
9. Separate the surface frame from the main body of the notebook.
10. Place the surface frame upside down. Remove the four screws fastening the touchpad board and separate it from the surface frame.

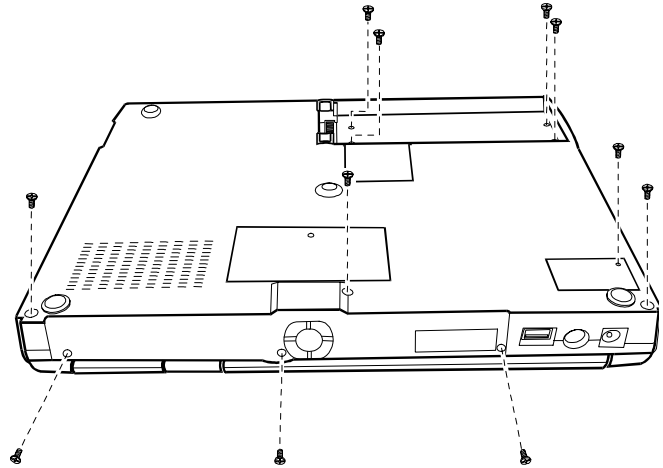


Figure 7-28. Removing Bottom Screws and Rear Side Screws

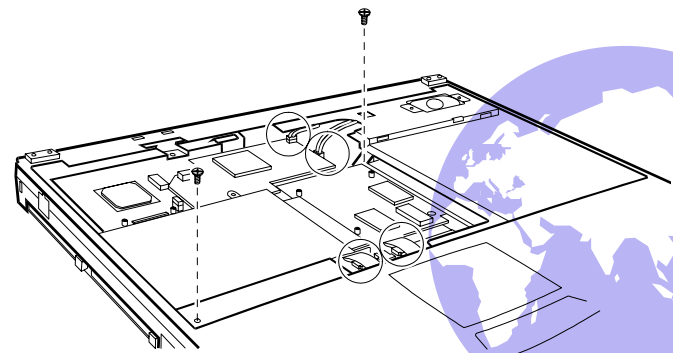


Figure 7-29. Removing the Surface Frame Screws and Connectors

7.2 System Disassembly

1. Fit the touchpad board into position. Replace the four screws securing the touchpad board. (Refer to Figure 7-30 earlier.)
2. Replace the surface frame. Reconnect touchpad cables and audio onnectors and replace the screws fastening the frame. (Refer to Figure 7-29 earlier.)
3. Place the notebook upside down. Replace eleven screws fixing the surface frame with the bottom board. (Refer to Figure 7-28 earlier.)
4. Replace the battery pack. (See section 7.2.1 Reassembly.)
5. Place the notebook surface up. Replace the LCD display. (See section 7.2.5 Reassembly.)
6. Replace the metal plate and secure with four screws. (See section 7.2.9 Reassembly step 2.)
7. Replace the keyboard and secure with three screws. (See section 7.2.8 Reassembly step 1 to 2.)
8. Replace the speaker panel and the two hinge covers. (See section 7.2.5 Reassembly step 2 to 3.)

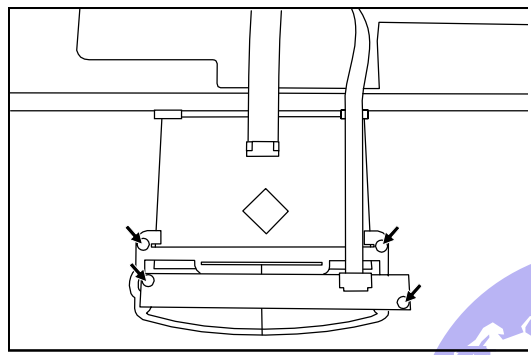


Figure 7-30. Removing the Four Screws Fastening the Touchpad Board

7.2 System Disassembly

7.2.13 System Board

- Disassembly

1. Remove the battery pack. (See section 7.2.1.)
2. Remove the CD-ROM drive. (See section 7.2.2.)
3. Remove the LCD assembly. (See section 7.2.5.)
4. Remove the CPU card. (See section 7.2.9.)
5. Remove the Data/Fax/Modem card if it exists. (See section 7.2.10.)
6. Remove the hard disk drive. (See section 7.2.11.)
7. Remove the surface frame. (See section 7.2.12.)
8. Unplug the VGA board from the system board.
9. Remove one screw fastening the Audio/Charger board.
10. Unplug the Audio/Charger board from the system board
11. Remove four screws fastening the system board.
12. Unplug the floppy disk drive cable from the floppy disk.

Lift the system board free.

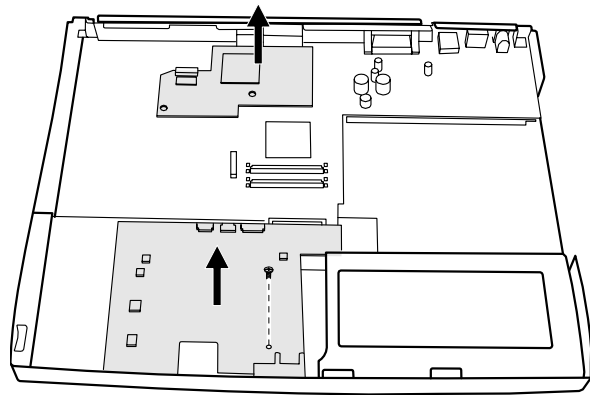


Figure 7-31. Removing VGA Board and Audio/Charger Board

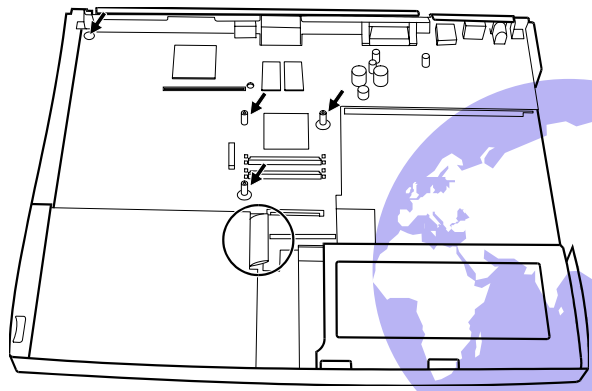


Figure 7-32. Removing System Board Screws and Unplugging the Floppy Disk Drive Cable

7.2 System Disassembly

- Reassembly

1. Fit the system board into place.
2. Connect the floppy disk drive cable to the floppy disk and secure the system board with four screws. (Refer to Figure 7-32 earlier.)
3. Replace the Audio/Charger board and secure with one screw.
4. Replace the VGA board by plugging the connector to the system board. (Refer to Figure 7-31 earlier.)
5. Replace the touchpad board and reconnect the audio connectors. (See section 7.2.12 Reassembly)
6. Replace the hard disk drive with its bracket by plugging the connector to the system board and securing with two screws. (See section 7.2.11 Reassembly.)
7. Fit the Fax/Modem/Voice Card (if exist) into place and secure with two screws. (See section 7.2.10 Reassembly.)
8. Replace the CPU card. (See section 7.2.9 Reassembly.)
9. Replace the metal plate and secure with four screws. (See section 7.2.9 Reassembly step 2.)
10. Replace the keyboard and secure with three screws. (See section 7.2.8 Reassembly step 1 to 2.)
11. Attach the LCD assembly to the base unit and secure with four screws. (See section 7.2.5 Reassembly.)
12. Replace the speaker panel and the two hinge covers. (See section 7.2.5 Reassembly step 2 to 3.)
13. Replace the CD-ROM drive by sliding it into the compartment, plugging the connector, and secure with one bottom screw. (See section 7.2.2 Reassembly.)
14. Replace the battery pack. (See section 7.2.1 Reassembly.)

7.2 System Disassembly

7.2.14 Floppy Disk Drive

●Disassembly

1. Remove the system board. (See section 7.2.13 Disassembly.)
2. Remove the floppy disk drive by removing one screw and lifting the rear end of the floppy disk drive.

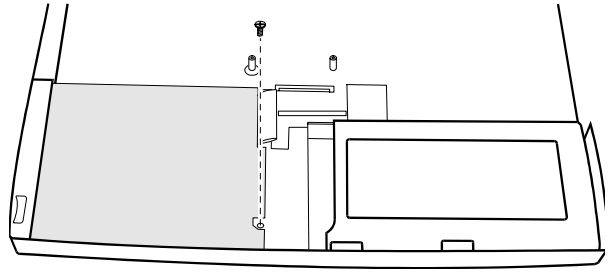


Figure7-33. Removing the Screw Fastening the Floppy Disk Drive

●Reassembly

1. Connect the floppy disk drive cable to the floppy disk drive and fit the floppy disk drive into place.
2. Secure the floppy disk with one screw. (Refer to Figure 7-33)
3. Replace the system board. (See section 7.2.13 Reassembly.)

8. MAINTENANCE DIAGNOSTICS

8.1 INTRODUCTION

EACH TIME THE COMPUTER IS TURNED ON, THE SYSTEM BIOS RUNS A SERIES OF INTERNAL CHECKS ON THE HARDWARE. THIS POWER-ON SELF TEST (POST) ALLOWS THE COMPUTER TO DETECT PROBLEMS AS EARLY AS THE POWER-ON STAGE. ERROR MESSAGES OF POST CAN ALERT YOU TO THE PROBLEMS OF YOUR COMPUTER.

IF AN ERROR IS DETECTED DURING THESE TESTS, YOU WILL SEE AN ERROR MESSAGE DISPLAYED ON THE SCREEN. IF THE ERROR OCCURS BEFORE THE DISPLAY IS INITIALIZED,THEN THE SCREEN CANNOT DISPLAY THE ERROR MESSAGE. ERROR CODES OR SYSTEM BEEPS ARE USED TO IDENTIFY A POST ERROR THAT OCCURS WHEN THE SCREEN IS NOT AVAILABLE.

THE VALUE FOR THE DIAGNOSTIC PORT (378H) IS WRITTEN AT THE BEGINNING OF THE TEST. THEREFORE, IF THE TEST FAILED, THE USER CAN DETERMINE WHERE THE PROBLEM OCCURRED BY READING THE LAST VALUE WRITTEN TO PORT 378H BY THE PIO DEBUG BOARD PLUG AT PIO PORT.

8.2 ERROR CODES

FOLLOWING IS A LIST OF ERROR CODES IN SEQUENCE DISPLAY ON THE PIO DEBUG BOARD.

CODE	BEEP	Description
00H		START OF BOOT LOADER SECQUENCE.
01H		DISABLE A20 THROUGH A20, NOT SEND.
02H	.._.	INITIALIZE CHIPSET OR BIOS NOT SHADOWED.
03H		PERFORM CONVENTIONAL RAM TEST WITH CROSSED-PATTERN R/W.
04H	._..	MOVE BOOT LOADER TO THE RAM OR BIOS CHECKSUM BAD.
05H		START POINT OF EXECUTION OF BOOT LOADER IN RAM.
06H		PERFORM PNP INITIALIZATION FOR CRYSTAL AUDIO CHIP OR CHECK
		OVERRIDE OPTION, NOT SEND.
07H		SHADOW SYSTEM BIOS.
08H		CHECKSUM SYSTEM BIOS ROM, NOT SEND.
09H		PROCEED WITH NORMAL BOOT.
0AH		PROCEED WITH CRISIS BOOT.
0FH	——	NO RAM OR DRAM SIZING.
10H		INITIAL L1, L2 CACHE, MAKE STACK AND DIAGNOSE CMOS.
11H		TURN OFF FAST A20 FOR FOR POST. RESET GDTS, 8259S QUICKLY.
12H		SIGNAL POWER ON RESET AT CMOS.
13H		INITIALIZE THE CHIPSET, (SDRAM).***SOLUTION: TRY TO CLEAR CMOS***
14H		SEARCH FOR ISA BUS VGA ADAPTER.
15H		RESET COUNTER/TIMER 1.
16H		USER REGISTER CONFIG THROUGH CMOS.
18H		DISPATCH TO 1ST 64K RAM TEST.
19H		CHECKSUM THE ROM.
1AH		RESET PIC'S(8259).
1BH		INITIALIZE VIDEO ADAPTER(S).
1CH		INITIALIZE VIDEO (6845 REGS).
1DH		INITIALIZE COLOR ADAPTER.
1EH		INITIALIZE MONOCHROME ADAPTER.
1FH		TEST 8237A PAGE REGISTERS.
20H		PERFORM KEYBOARD SELF TEST.
21H		TEST & INITIALIZE KEYBOARD CONTROLLER.
22H		CHECK IF CMOS RAM VALID.
23H		TEST BATTER FAIL & CMOS X-SUM.
24H		TEST THE DMA CONTROLLER.
25H		INITIALIZE 8237A CONTROLLER.
26H		INITIALIZE INTERRUPT VECTORS TABLE.
27H		RAM QUICK SIZING.

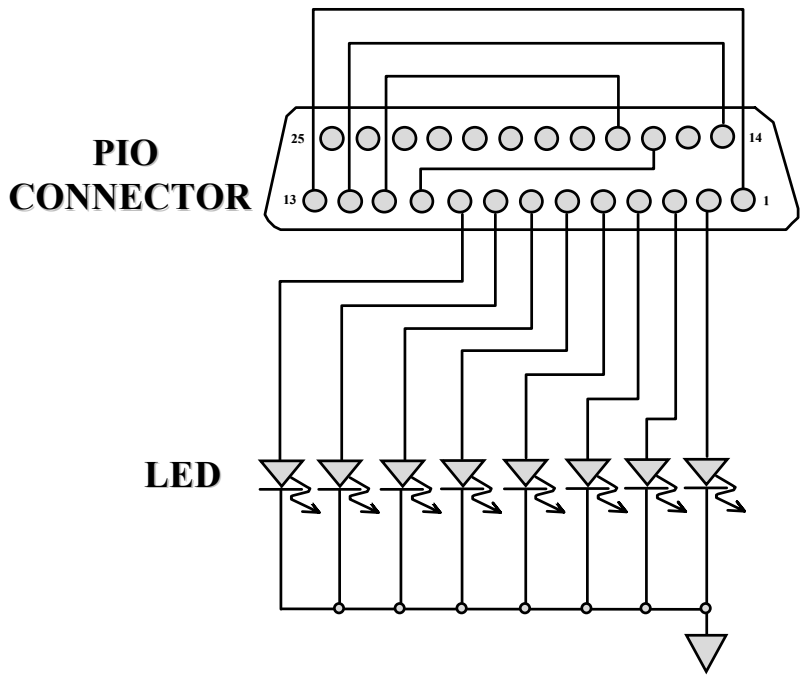
CODE	BEEP	Description
28H		PROTECTED MODE ENTERED SAFELY.
29H		RAM TEST COMPLETED.
2AH		PROTECTED MODE EXIT SUCCESSFUL .
2BH		SETUP SHADOW.
2CH		PREPARE TO INITIALIZE VIDEO.
2DH		SEARCH FOR MONOCHROME ADAOTER.
2EH		SEARCH FOR COLOR ADAPTER, VGA INITIALIZE.
2FH		SIGN-ON MESSAGES DISPLAYED.
30H		SPECIAL INIT OF KEYBOARD CONTROLLER.
31H		TEST IF KEYBOARD PRESENT.
32H		TEST KEYBOARD INTERRUPT.
33H		TEST KEYBOARD COMMAND BYTE.
34H		TEST, BLANK AND COUNT ALL RAM.
35H		PROTECTED MODE ENTERED SAFELY(2).
36H		RAM TEST COMPLETED.
37H		PROTECTED MODE EXIT SUCCESSFUL .
38H		UPDATE KEYBOARD OUTPUT PORT TO DISABLE GATE OF A20.
39H		SETUP CACHE CONTROLLER.
3AH		TEST IF 18.2HZ PERIODIC WORKING.
3BH		INITIALIZE BIOS DATA AREA AT 40:0.
3CH		INITIALIZE THE HARDWARE INTERRUPT VECTOR.
3DH		SEARCH AND INIT THE MOUSE.
3EH		UPDATE NUMLOCK STATUS.
3FH		OEM INITIALIZATION OF COMM AND LPT PORTS.
40H		CONFIGURE THE COMM AND LPT PORTS.
41H		INITIALIZE THE FLOPPIES.
42H		INITIALIZE THE HARD DISK.
43H		INITIALIZE ADDITIONAL ROMS.
44H		OEM'S INIT OF POWER MANAGEMENT, (CHECK SMI).
45H		UPDATE NUMLOCK STATUS.
46H		TEST FOR COPROCESSOR INSTALLED.
47H		OEM FUNCTIONS BEFORE BOOT(PCMCIA, CARDBUSS).
48H		DISPATCH TO OPERATION SYSTEM BOOT.
49H		JUMP INTO BOOTSTRAP CODE.
4AH		OEM'S INIT OF PM WITH USB.
FO~F1H	....	RMA TEST FAILED.

8.3 PIO PORT (378H) DIAGNOSTIC TOOLS

8.3.1 PARTS USED:

- LED * 8
- PIO CONNECTOR * 1

8.3.2 CIRCUIT:



PIN1 : STROBE ⟷ PIN 13 : SLCT

PIN10: ACK# ⟷ PIN 16 : INT#

PIN11: BUSY ⟷ PIN 17 : SELIN#

PIN12: PTERR ⟷ PIN 14 : AUTOFD#

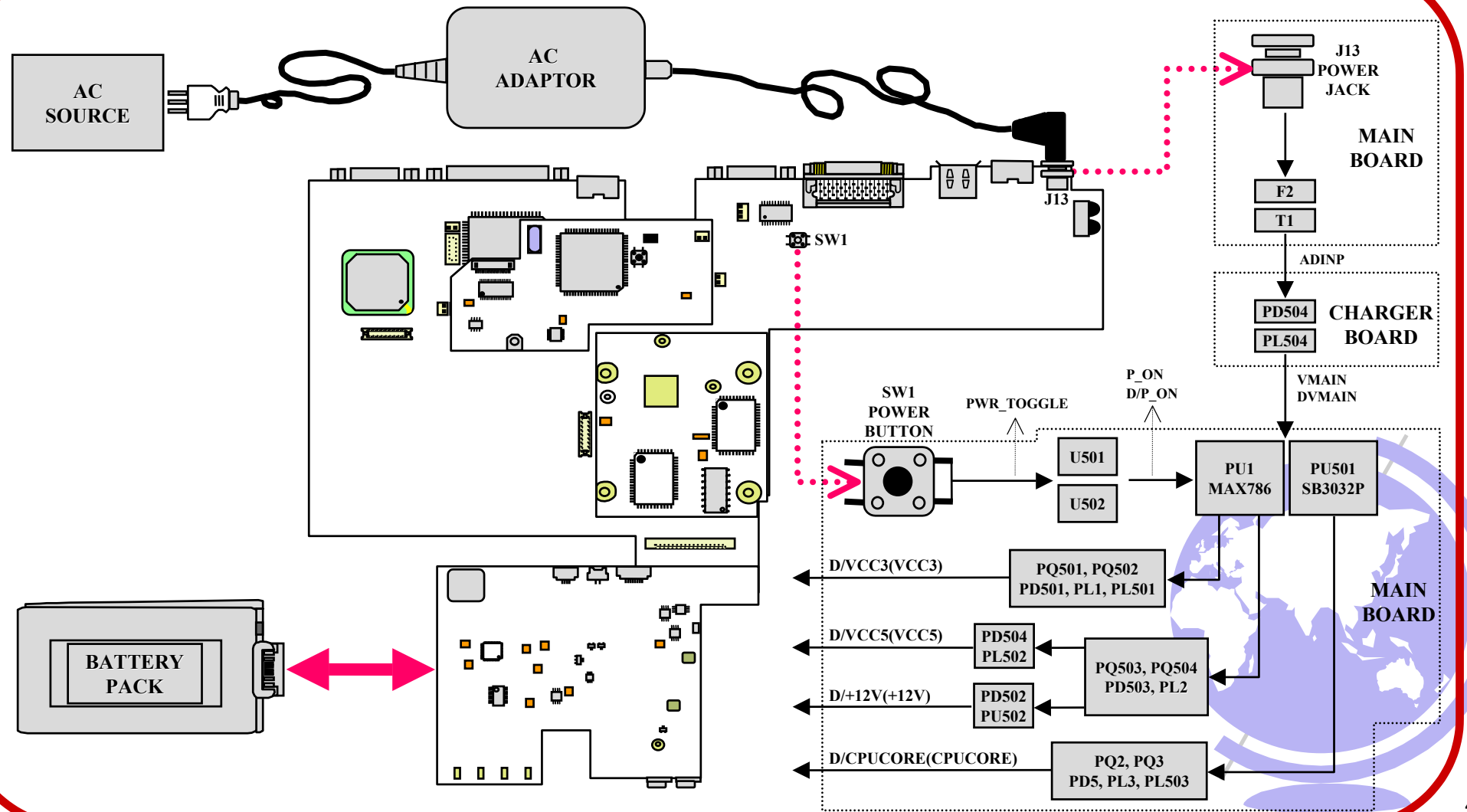
PIN{9:2}: PD{7:0}

9. TROUBLE SHOOTING

9.1 NO POWER

SYMPTOM:

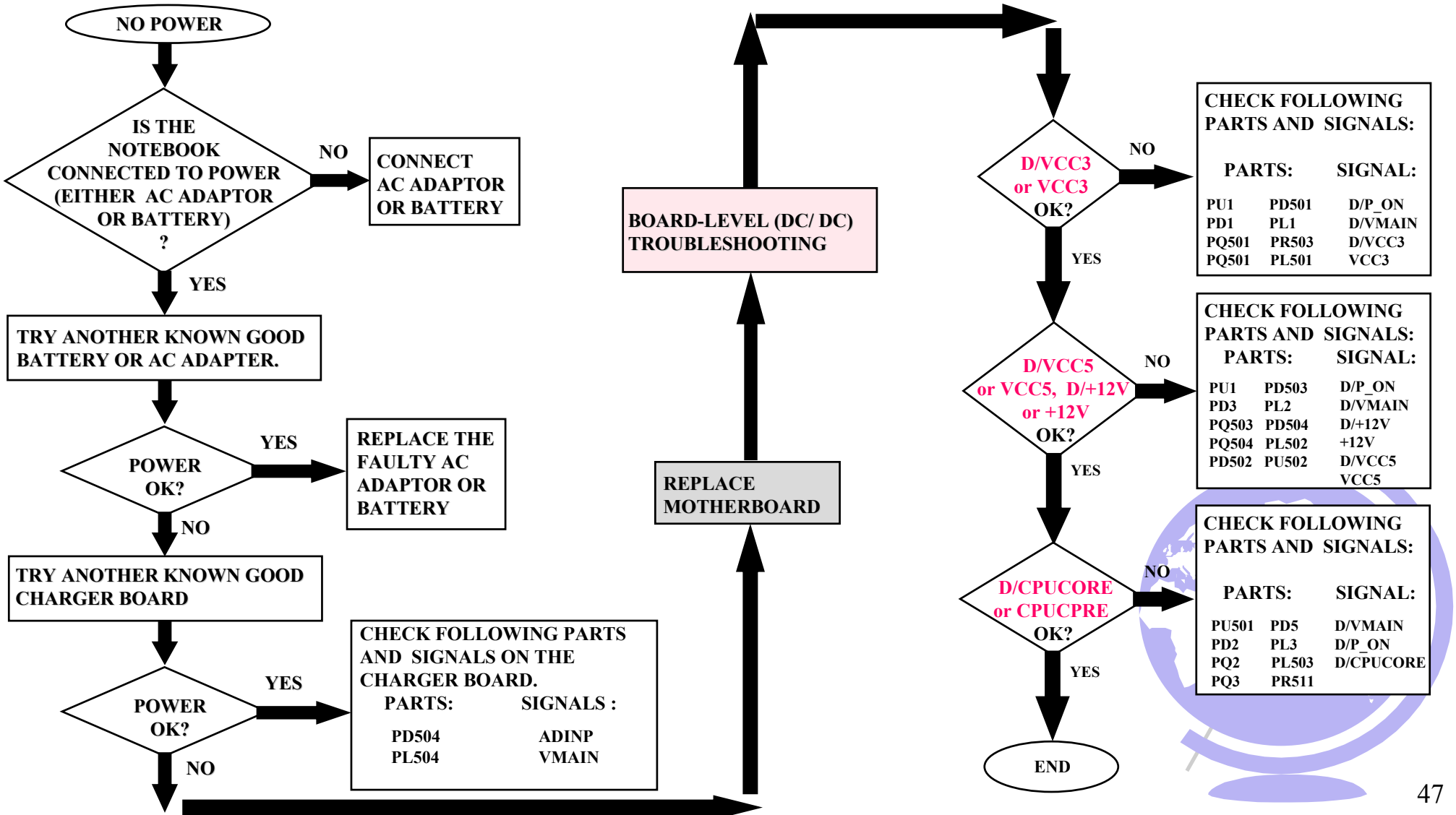
WHEN THE POWER BUTTON IS PRESSED, NOTHING HAPPENS, POWER INDICATOR IS NOT LIGHT UP.



9.1 NO POWER

SYMPTOM:

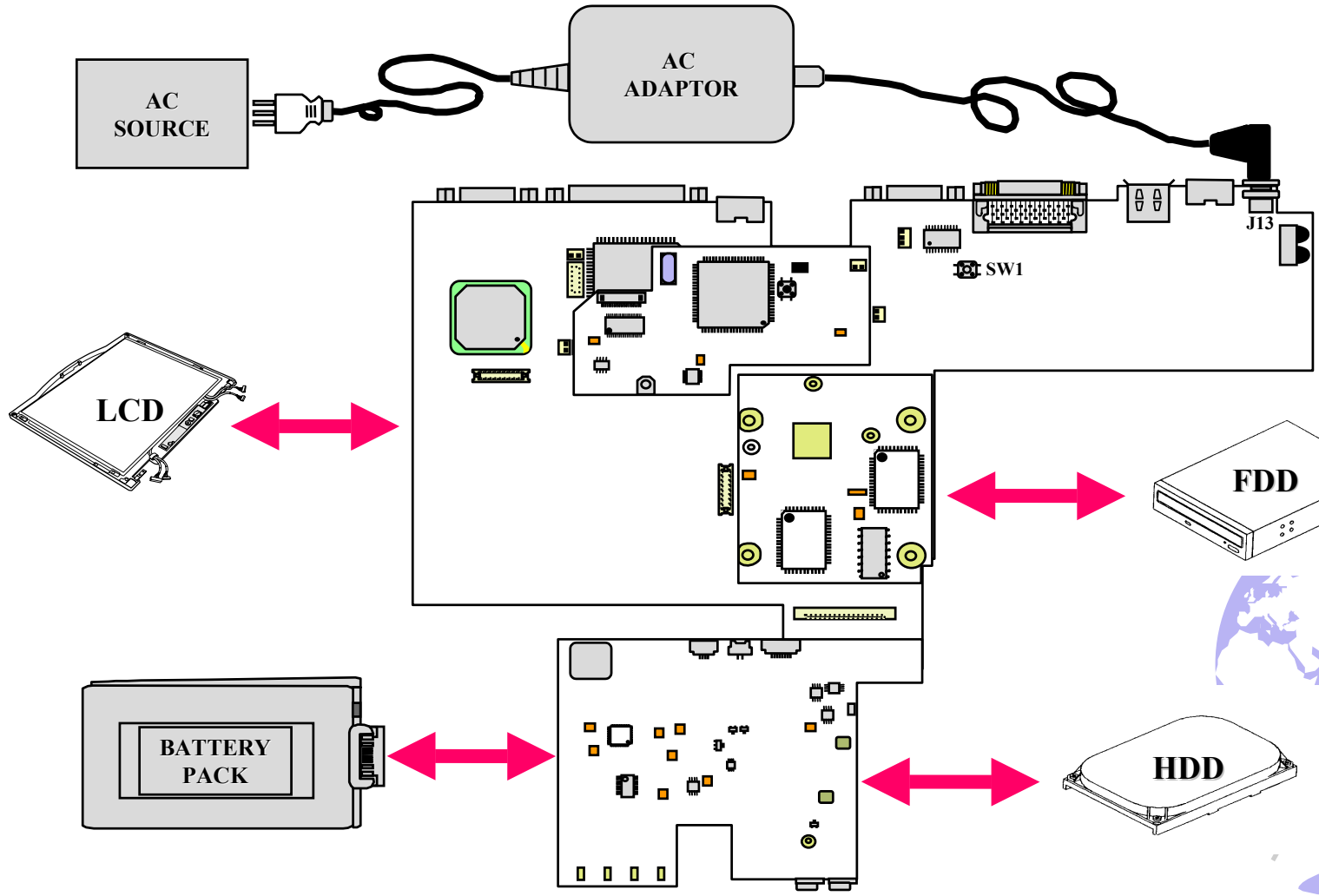
WHEN THE POWER BUTTON IS PRESSED, NOTHING HAPPENS, POWER INDICATOR IS NOT LIGHT UP.



9.2 NO DISPLAY (SYSTEM FAILURE)

SYMPTOM:

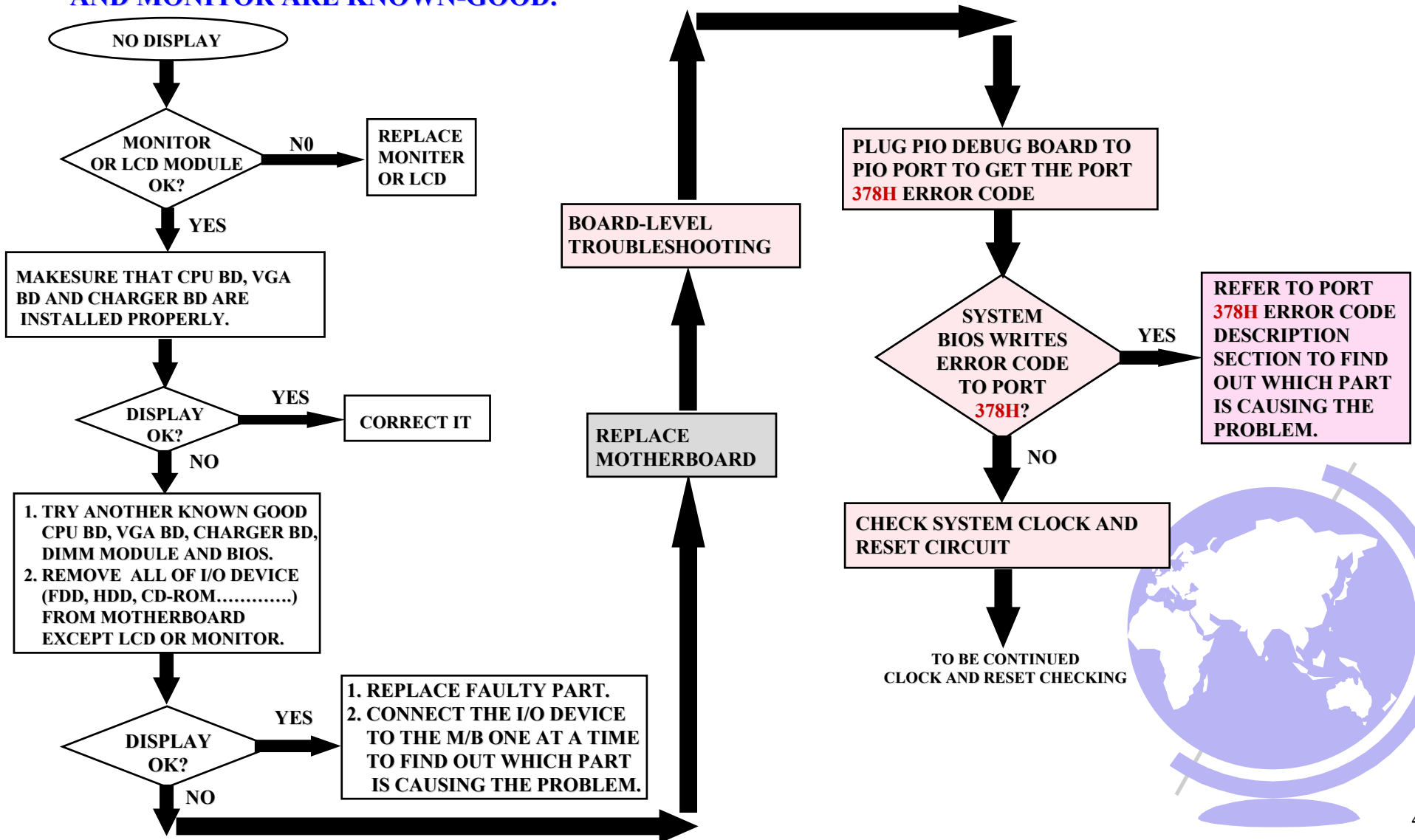
THERE IS NO DISPLAY ON BOTH LCD AND MONITOR AFTER POWER ON ALTHOUGH THE LCD AND MONITOR ARE KNOWN-GOOD.



9.2 NO DISPLAY (SYSTEM FAILURE)

SYMPTOM:

THERE IS NO DISPLAY ON BOTH LCD AND MONITOR AFTER POWER ON ALTHOUGH THE LCD AND MONITOR ARE KNOWN-GOOD.



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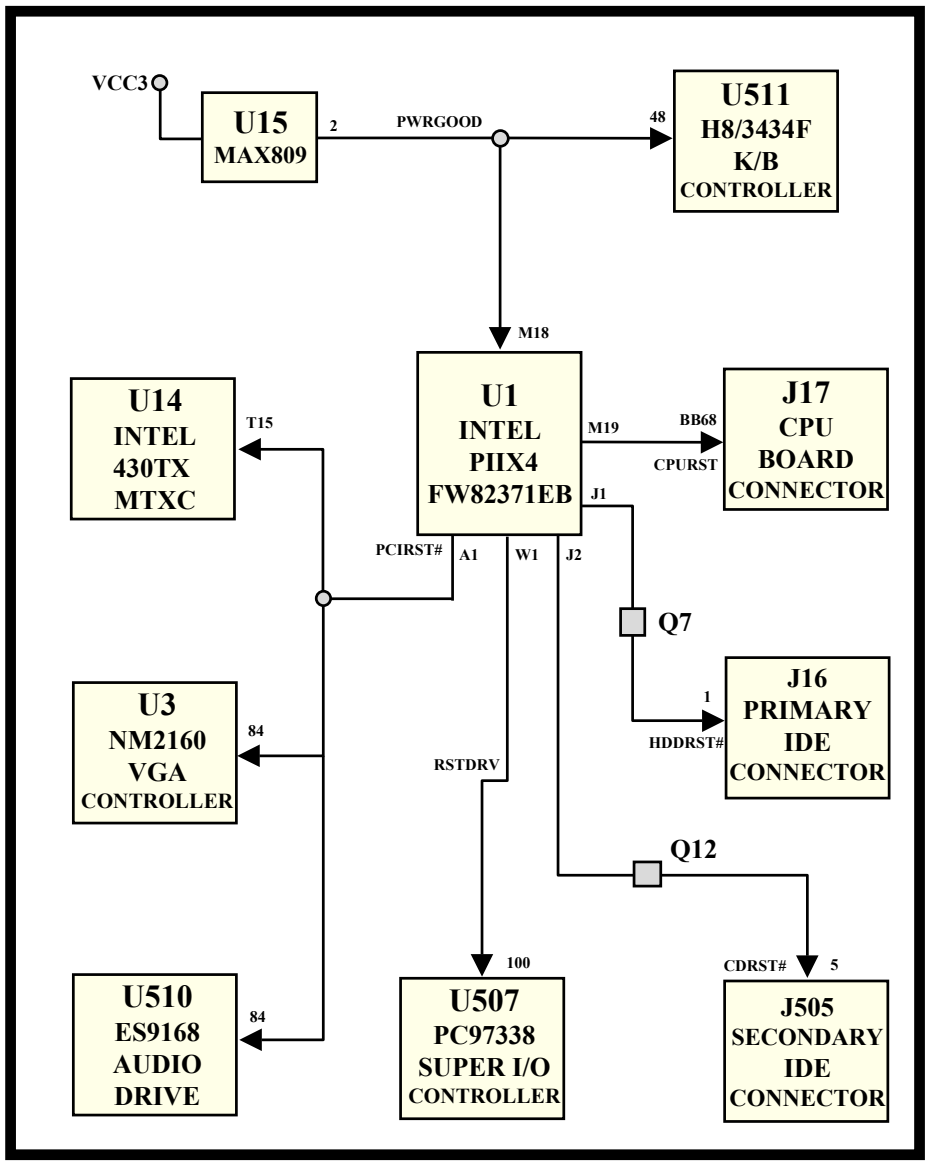
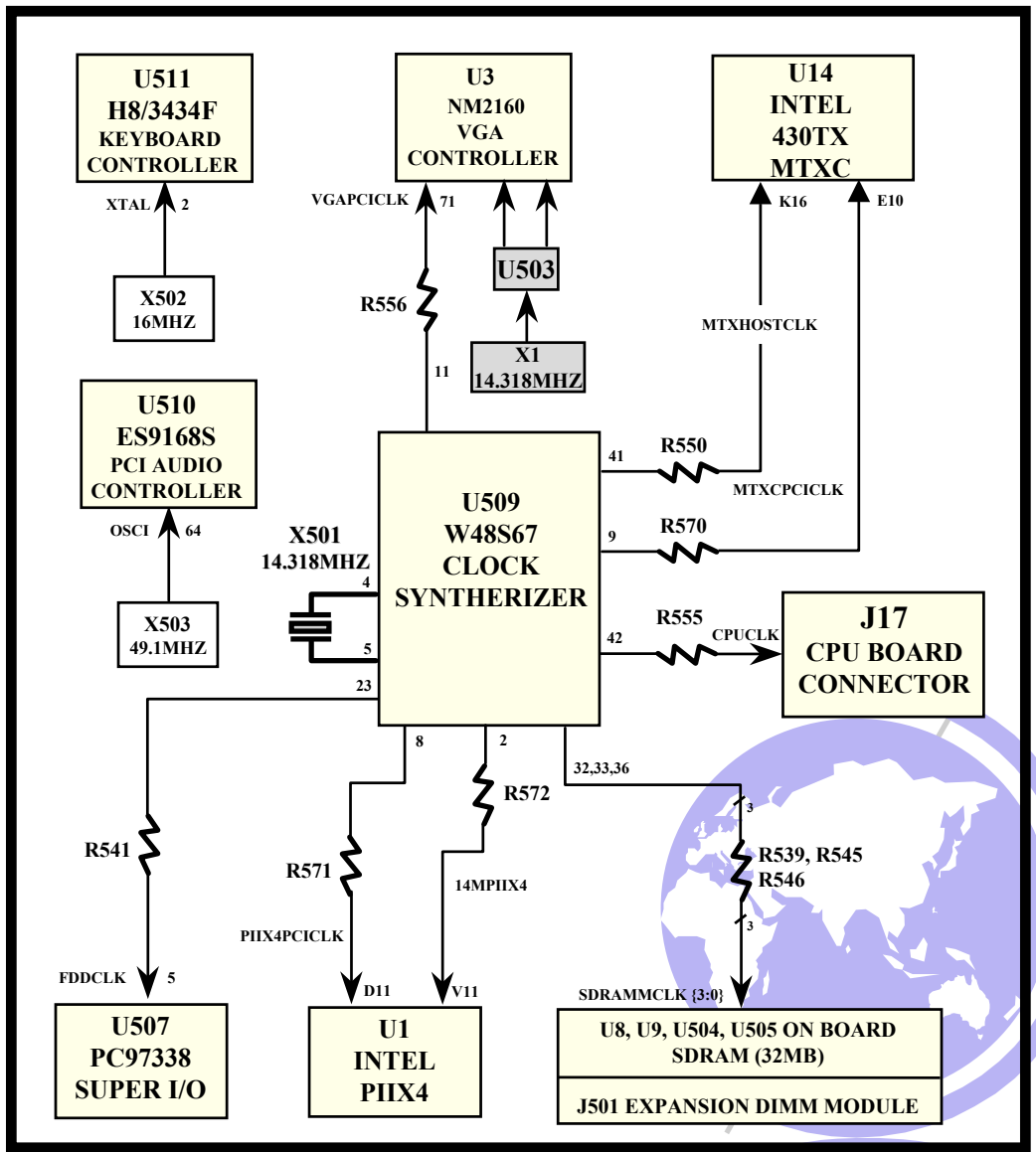
9.2 NO DISPLAY (SYSTEM FAILURE)

*******CLOCK AND RESET CIRCUIT CHECKING*******

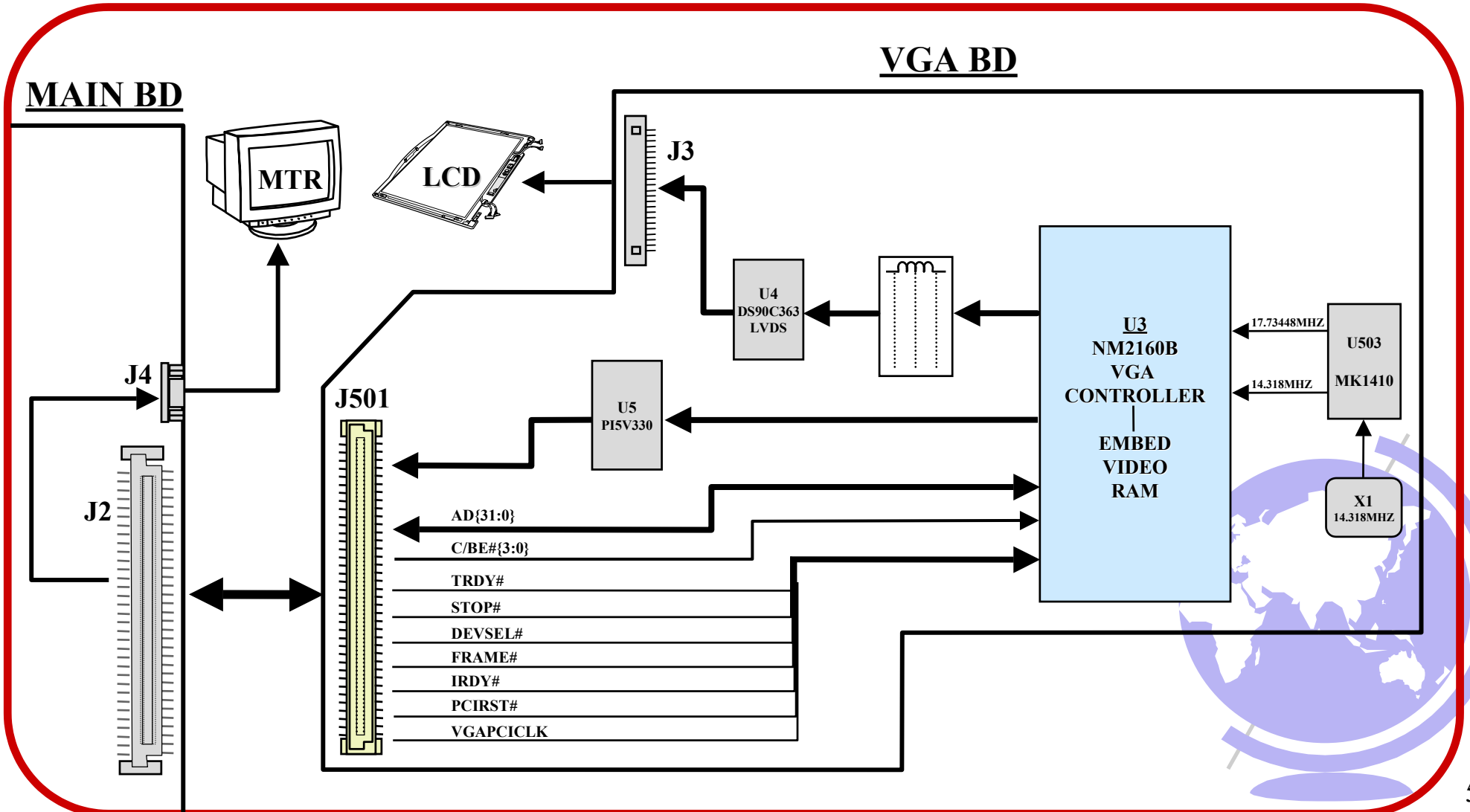




9.3 VGA CONTROLLER FAILURE

SYMPTOM:

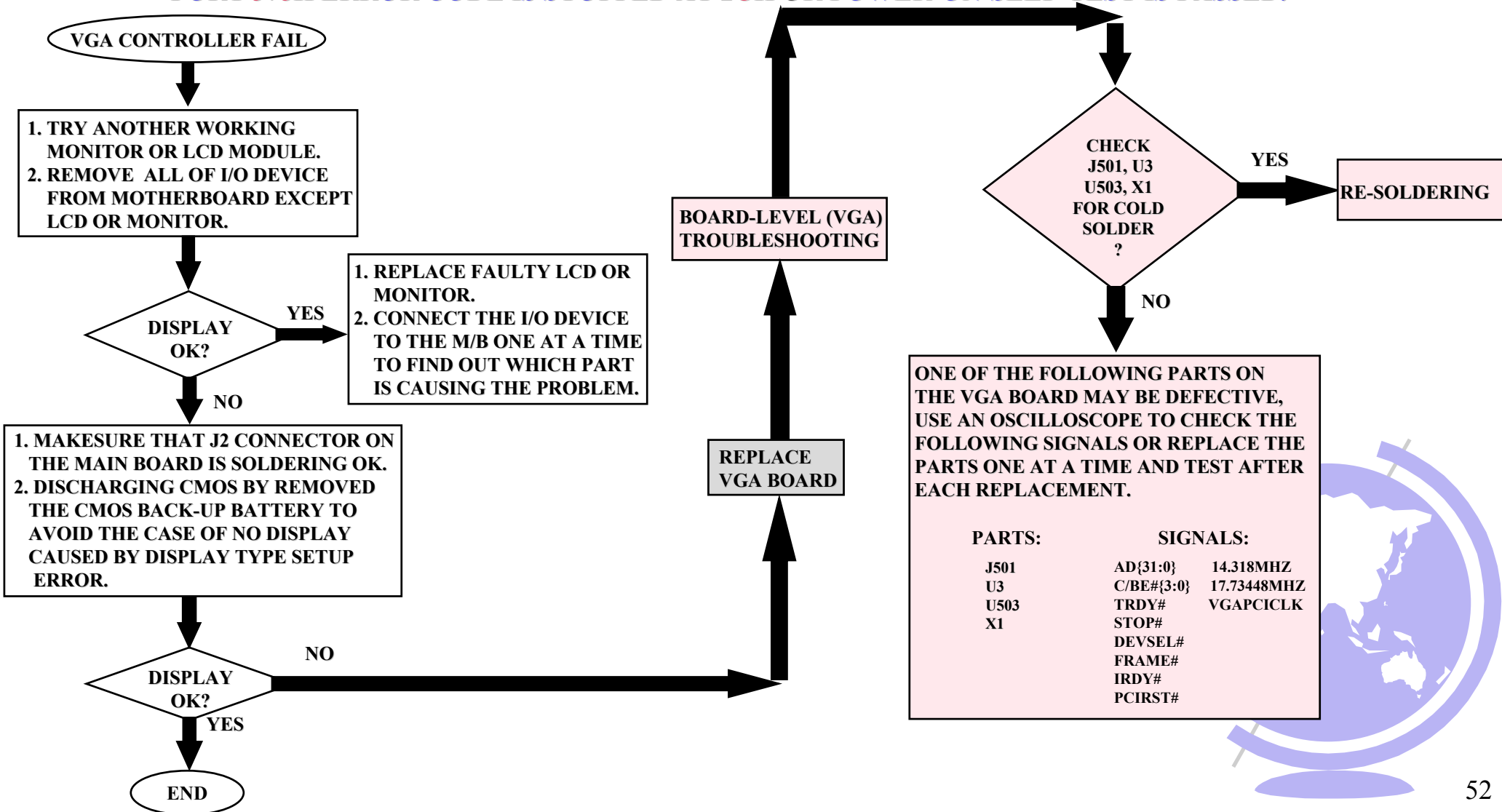
THERE IS NO DISPLAY ON BOTH LCD AND MONITOR AND THE PIO DEBUG BOARD SHOWS THE PORT 378H ERROR CODE IS STOPPED AT 2CH OR POWER-ON-SELF-TEST IS PASSED.



9.3 VGA CONTROLLER FAILURE

SYMPTOM:

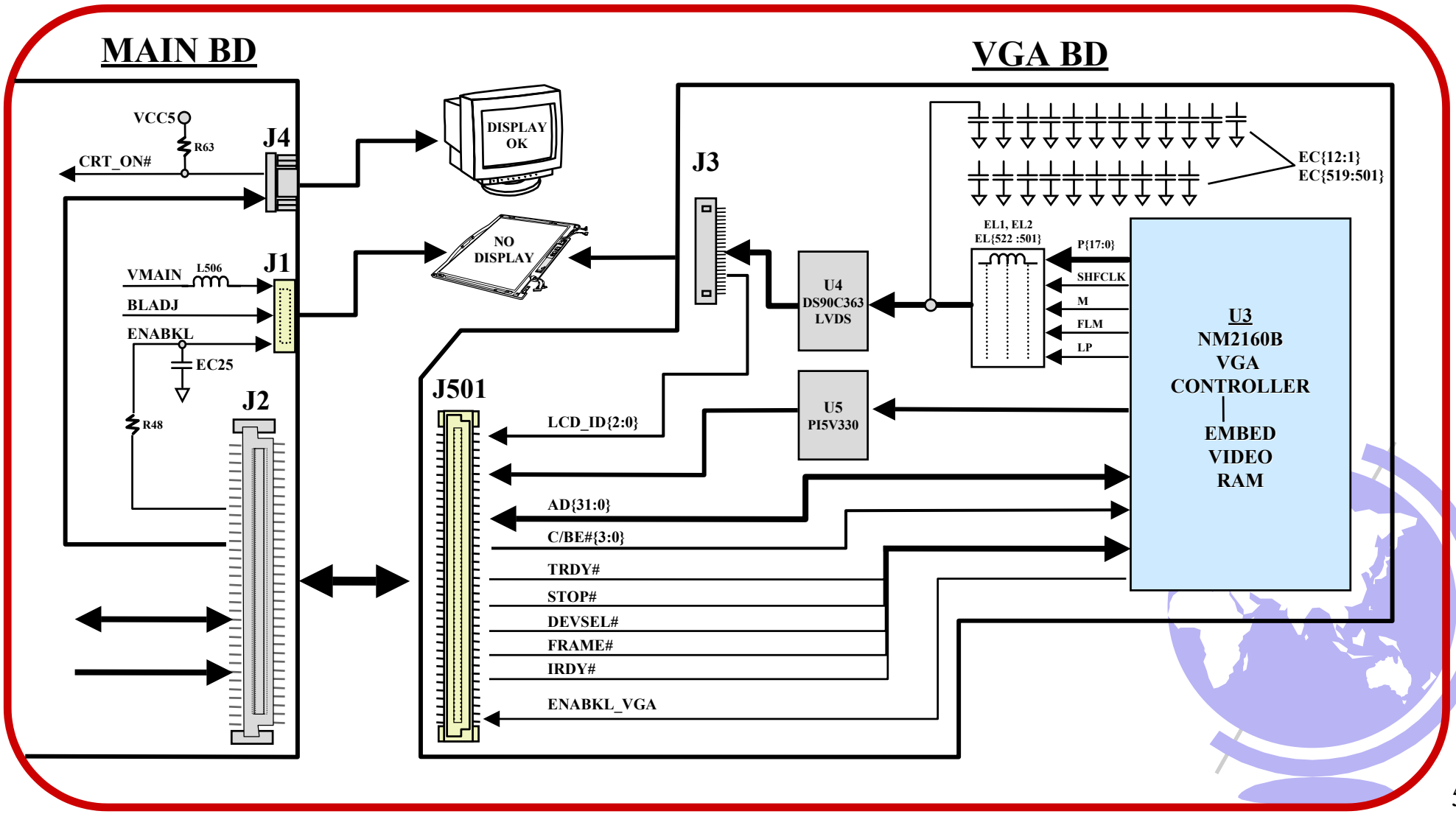
THERE IS NO DISPLAY ON BOTH LCD AND MONITOR AND THE PIO DEBUG BOARD SHOWS THE PORT 378H ERROR CODE IS STOPPED AT 2CH OR POWER-ON-SELF-TEST IS PASSED.



9.4 LCD NO DISPLAY OR PICTURE ABNORMAL

SYMPTOM:

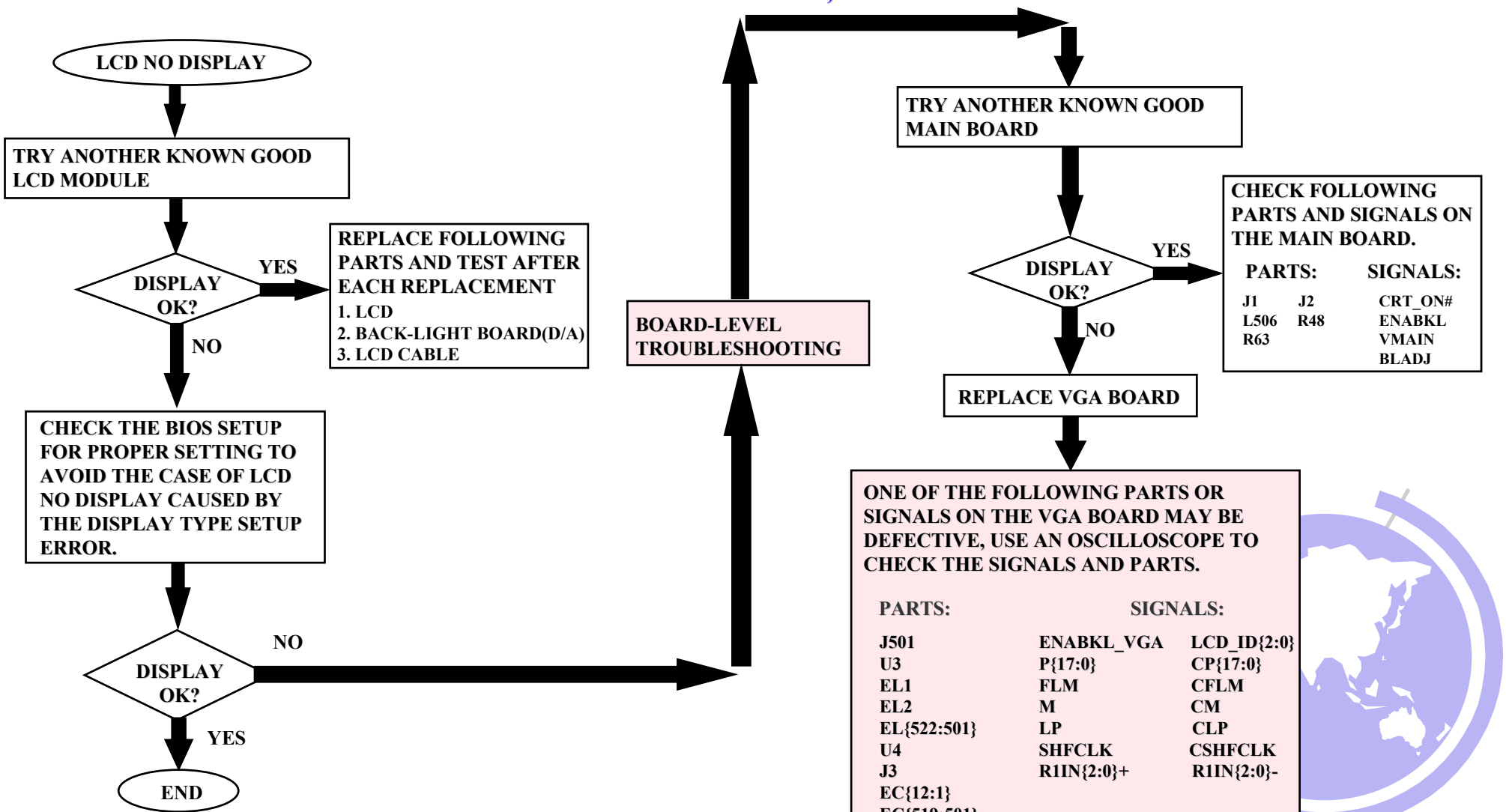
THE LCD SHOWS NOTHING OR ABNORMAL PICTURE, BUT IT IS OK FOR EXTERNAL MONITOR.



9.4 LCD NO DISPLAY OR PICTURE ABNORMAL

SYMPTOM:

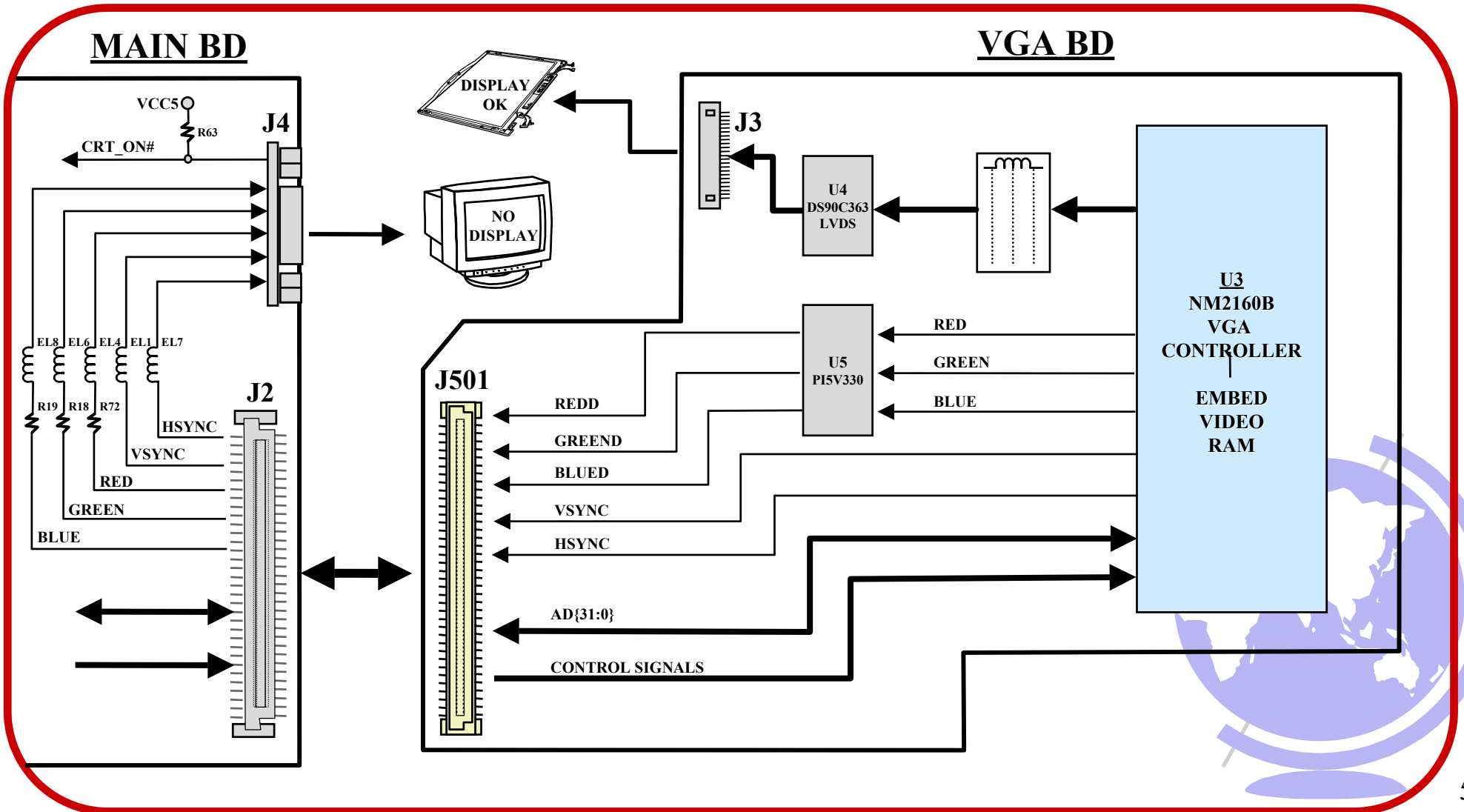
THE LCD SHOWS NOTHING OR ABNORMAL PICTURE, BUT IT IS OK FOR EXTERNAL MONITOR.



9.5 EXTERNAL MONITOR NO DISPLAY OR COLOR ABNORMAL

SYMPTOM:

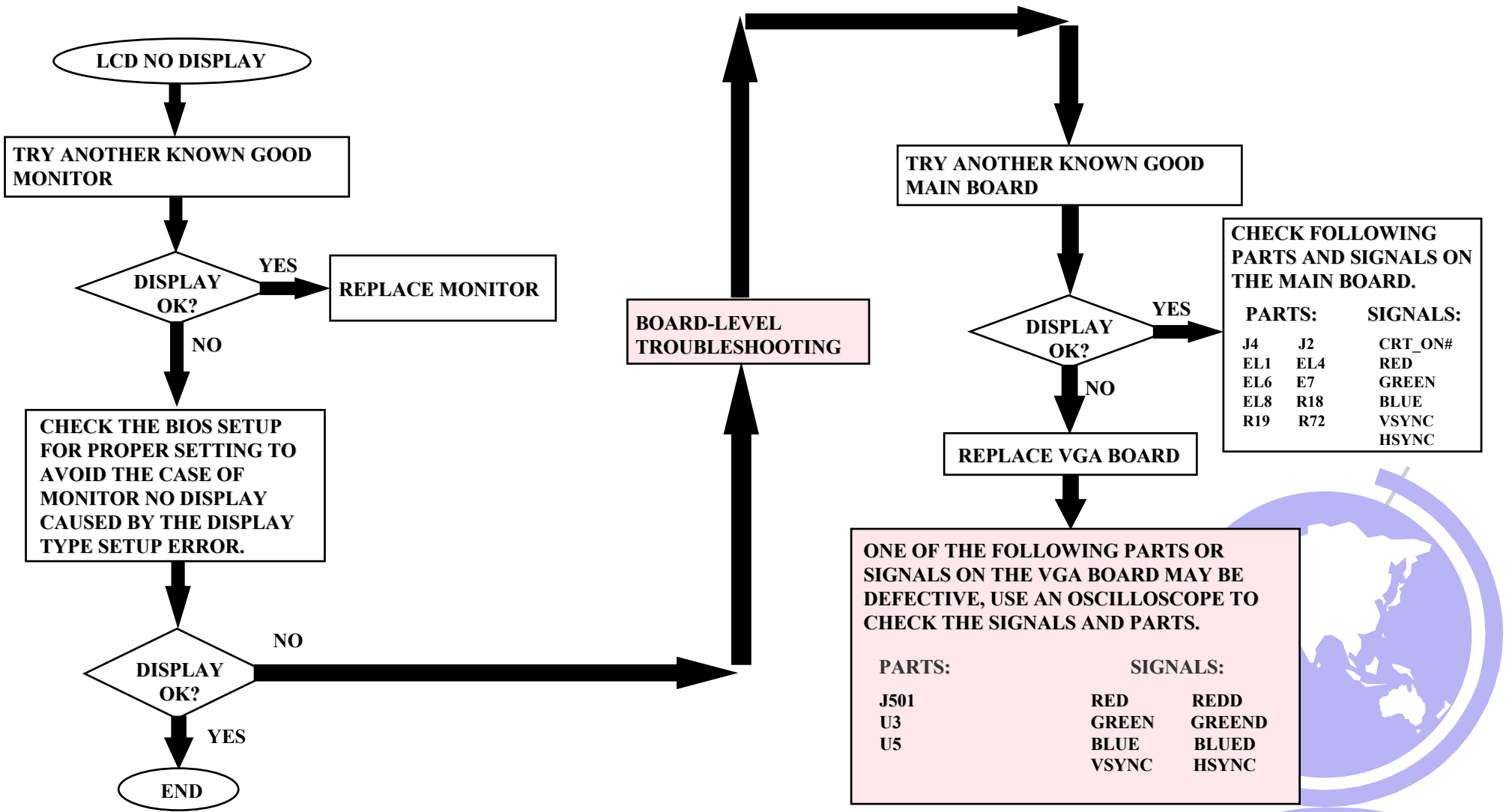
THE CRT MONITOR SHOWS NOTHING OR ABNORMAL COLOR, BUT IT IS OK FOR LCD.



9.5 EXTERNAL MONITOR NO DISPLAY OR COLOR ABNORMAL

SYMPTOM:

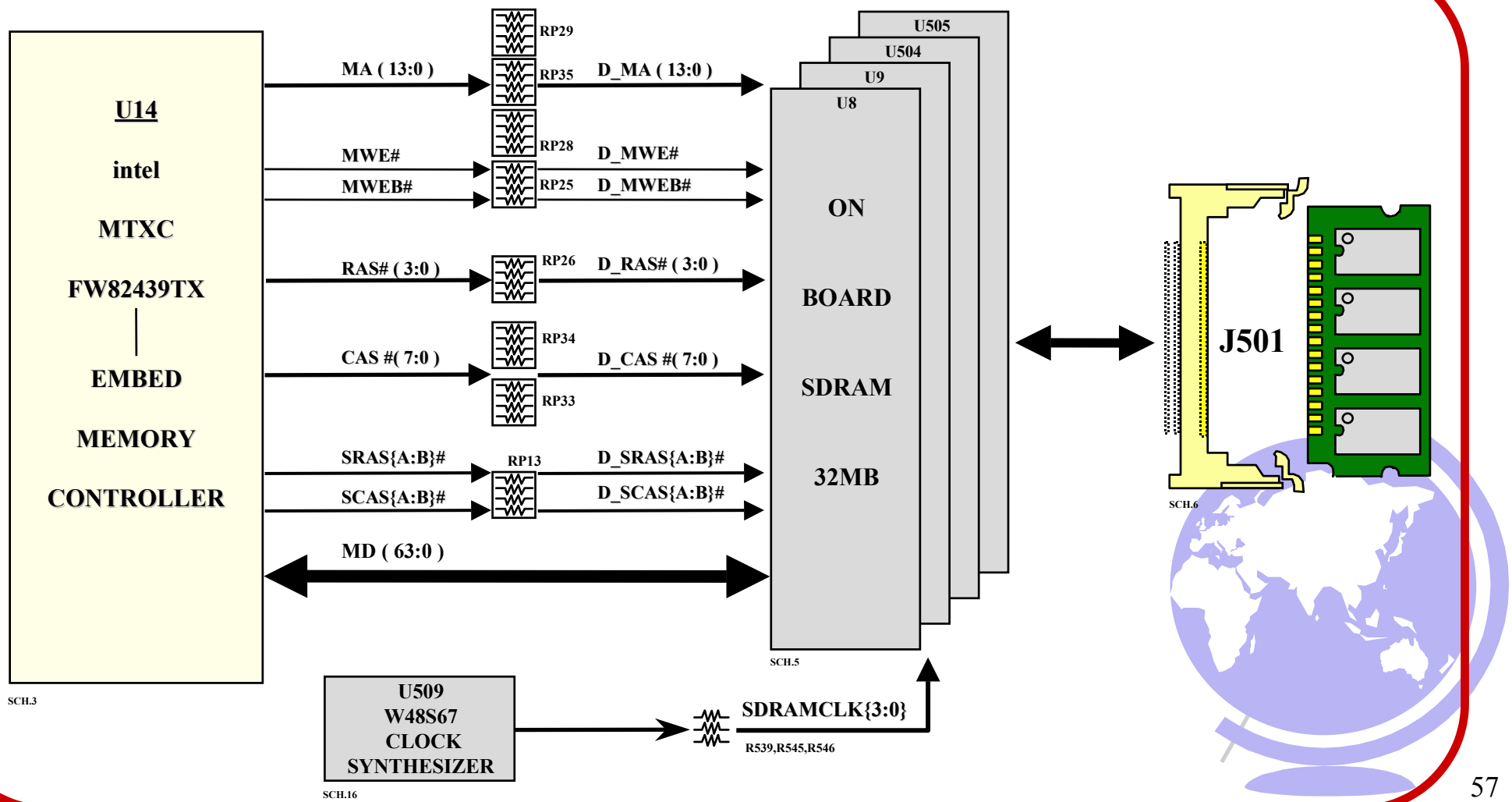
THE CRT MONITOR SHOWS NOTHING OR ABNORMAL COLOR, BUT IT IS OK FOR LCD.



9.6 MEMORY TEST ERROR

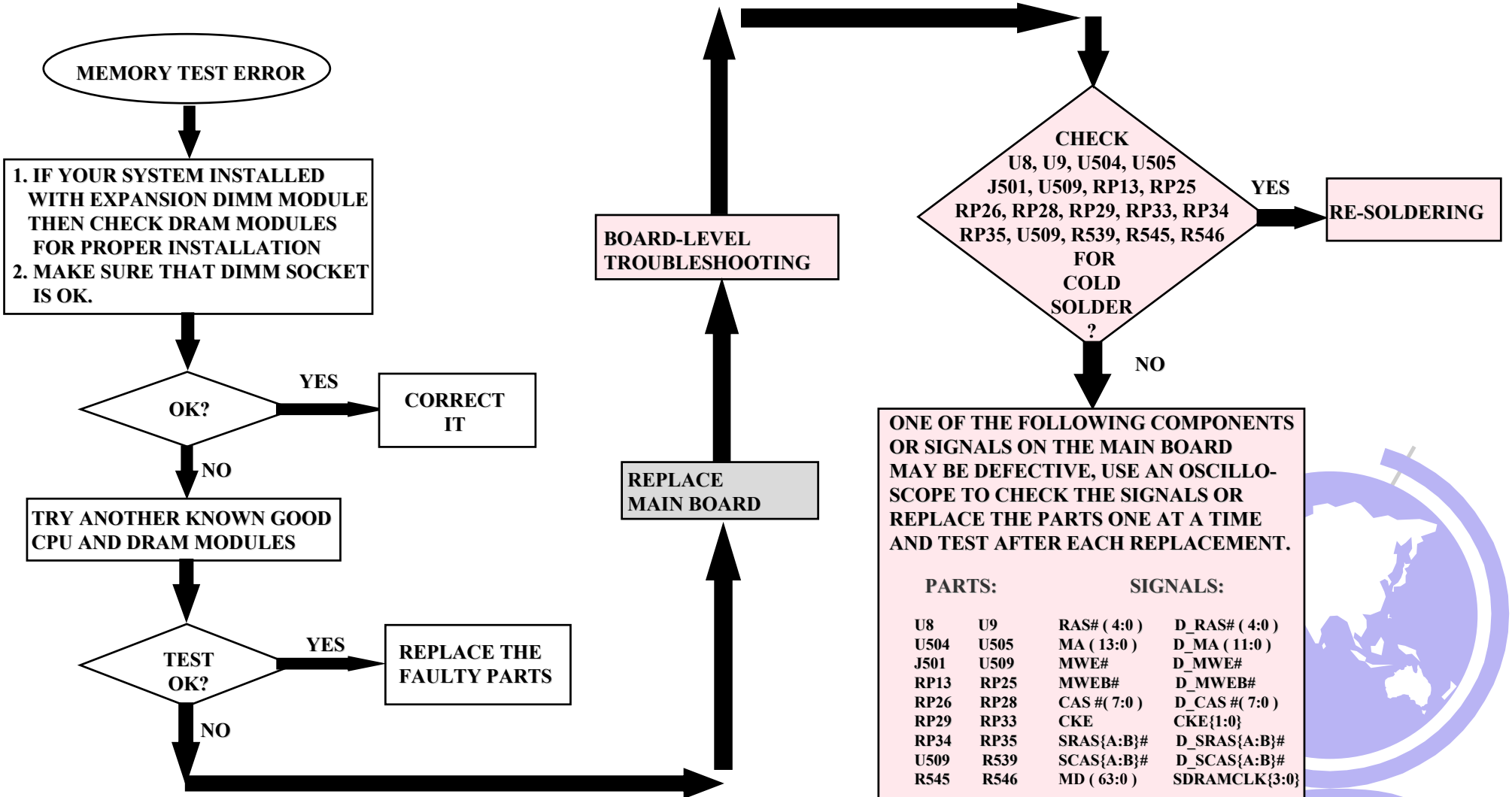
SYMPTOM:

PIO DEBUG BOARD SHOWS THE PORT 378H ERROR CODE IS STOPPED AT 0FH OR ERROR MESSAGE OF MEMORY FAILURE IS SHOWN.



9.6 MEMORY TEST ERROR

SYMPTOM:
PIO DEBUG BOARD SHOWS THE PORT 378H ERROR CODE IS STOPPED AT 0FH OR ERROR MESSAGE OF MEMORY FAILURE IS SHOWN.



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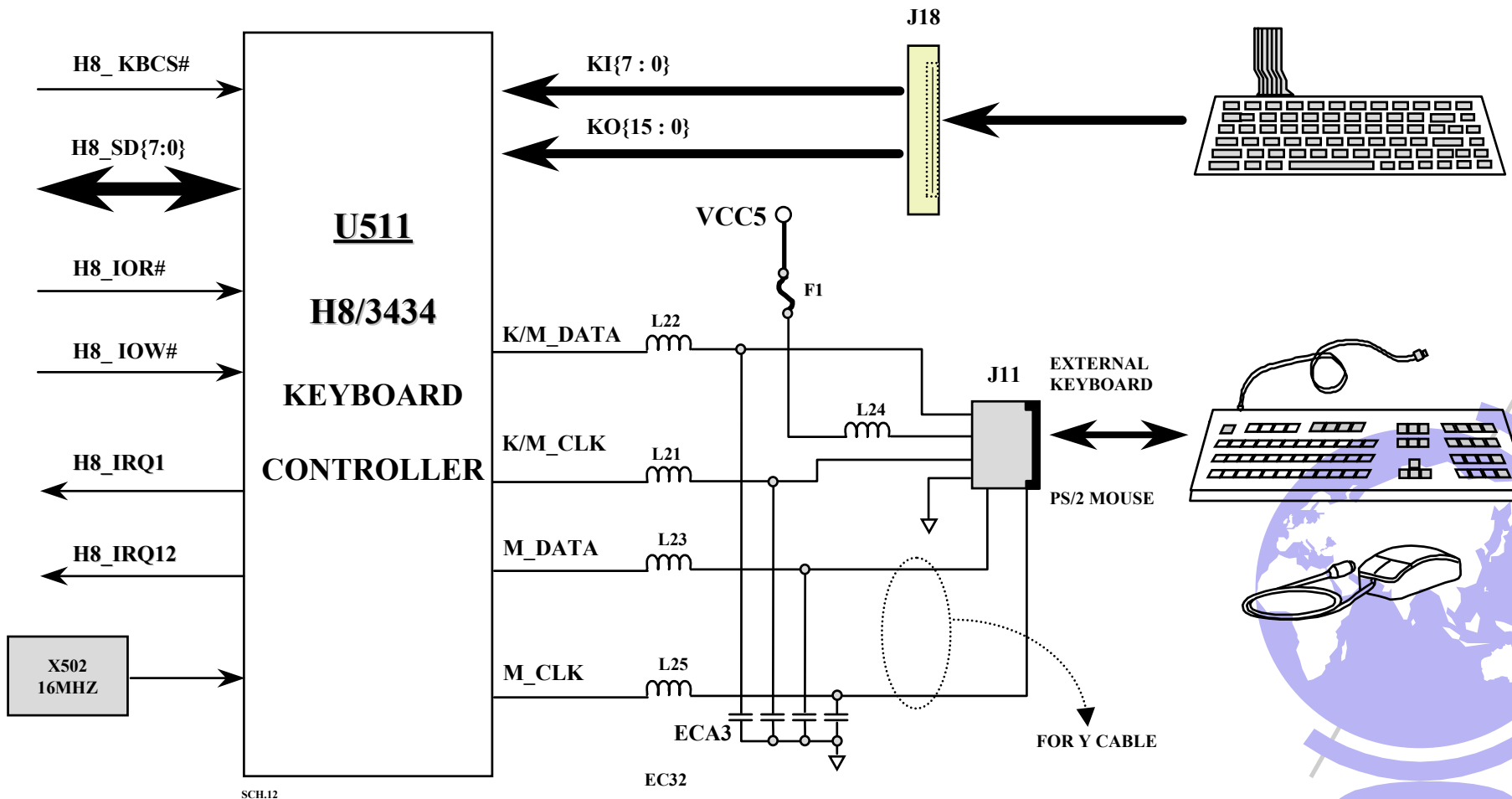
9.7 KEYBOARD TEST ERROR (INCLUDING EXTERNAL KEYBOARD & PS/2 MOUSE)

SYMPTOM:

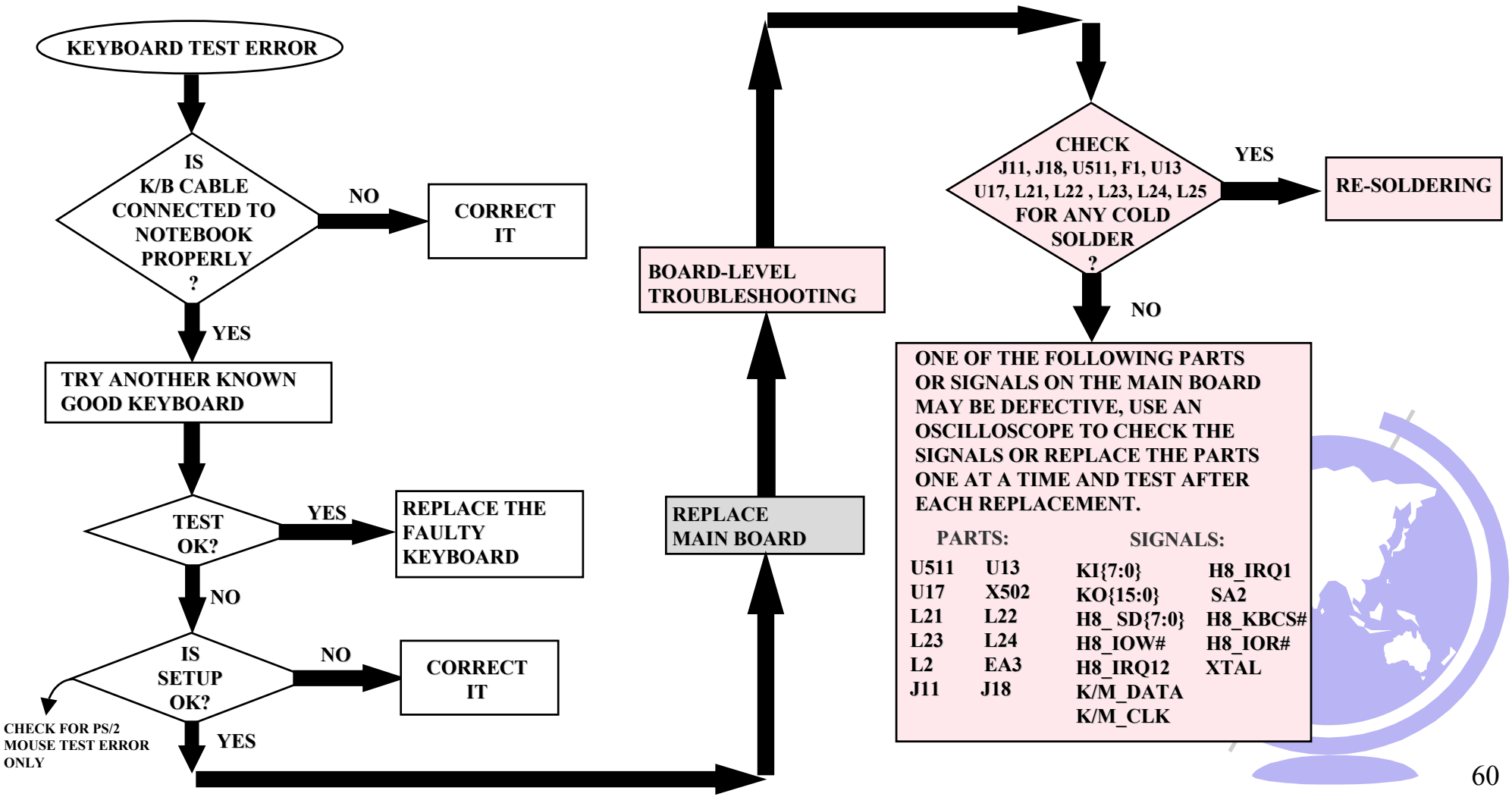
1. ERROR MESSAGE OF KEYBOARD FAILURE IS SHOWN OR ANY KEY DOESN'T WORK.
2. PIO DEBUG BOARD SHOWS THE PORT 378H ERROR CODE IS STOPPED AT 20H OR 21H.



9.7 KEYBOARD TEST ERROR (INCLUDING EXTERNAL KEYBOARD & PS/2 MOUSE)

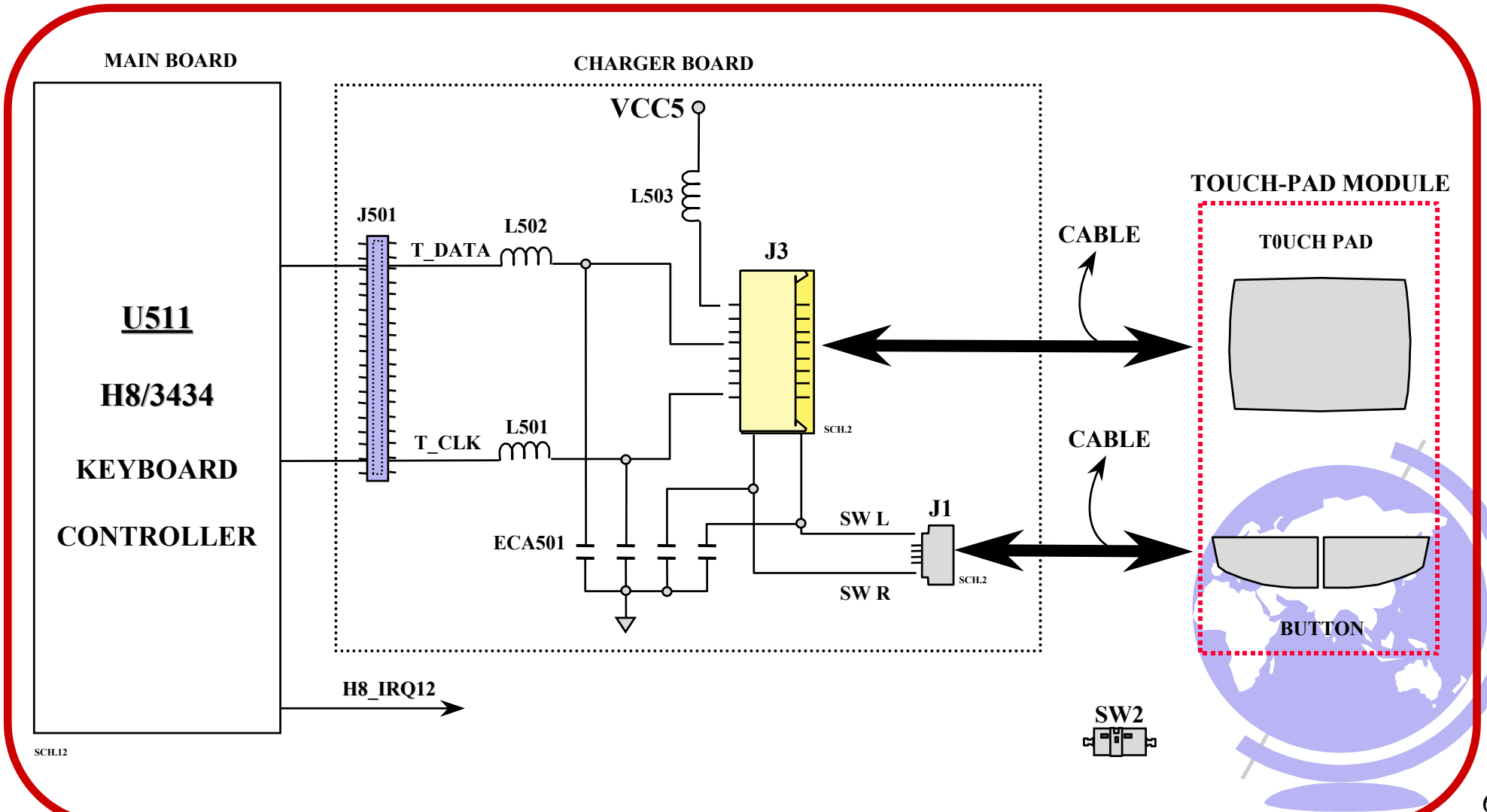
SYMPTOM:

1. ERROR MESSAGE OF KEYBOARD FAILURE IS SHOWN OR ANY KEY DOESN'T WORK.
2. PIO DEBUG BOARD SHOWS THE PORT 378H ERROR CODE IS STOPPED AT 20H OR 21H.



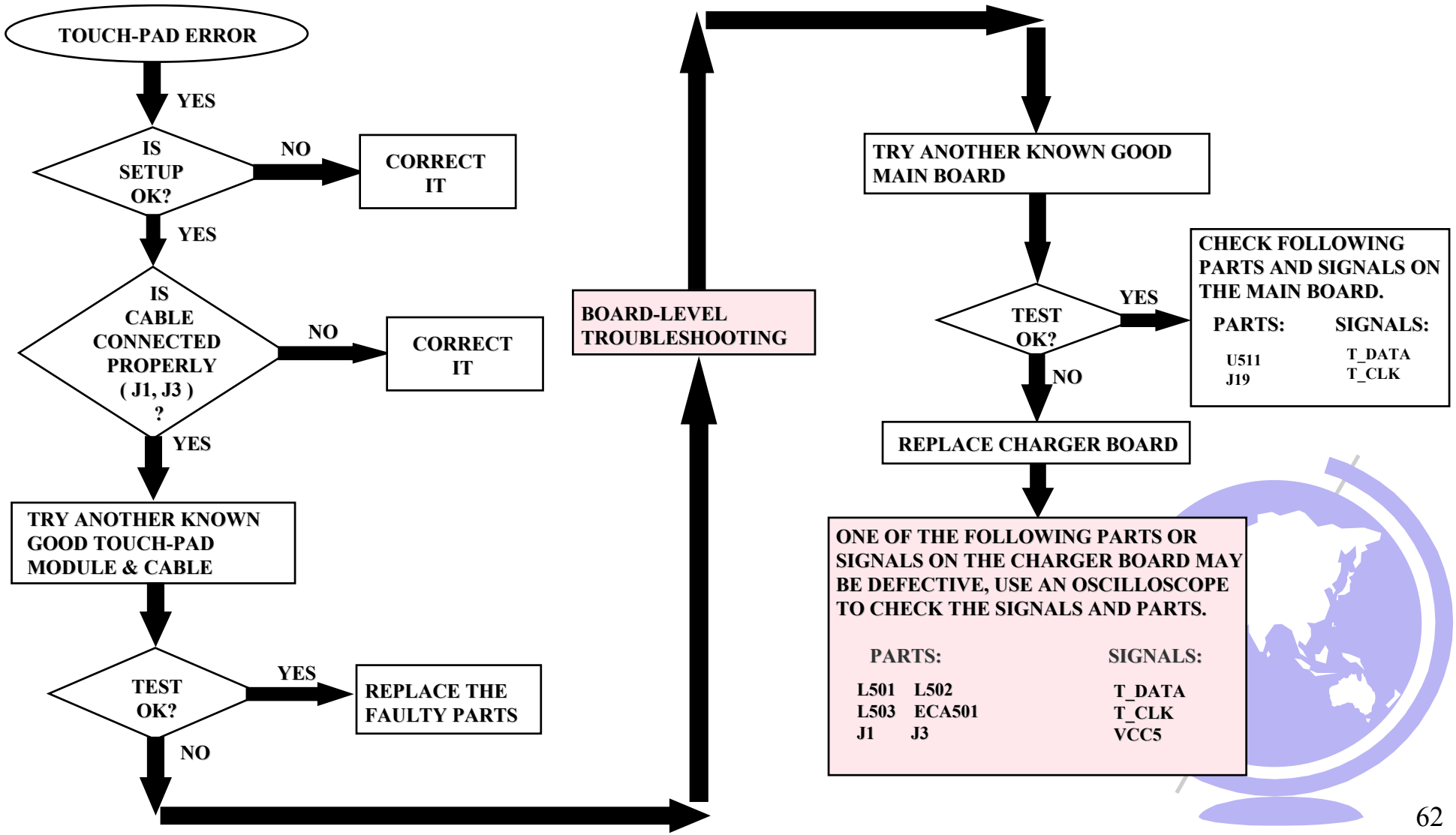
9.8 TOUCH-PAD TEST ERROR

SYMPTOM:
AN ERROR MESSAGE IS SHOWN WHEN THE TOUCH-PAD IS ENABLED.



9.8 TOUCH-PAD TEST ERROR

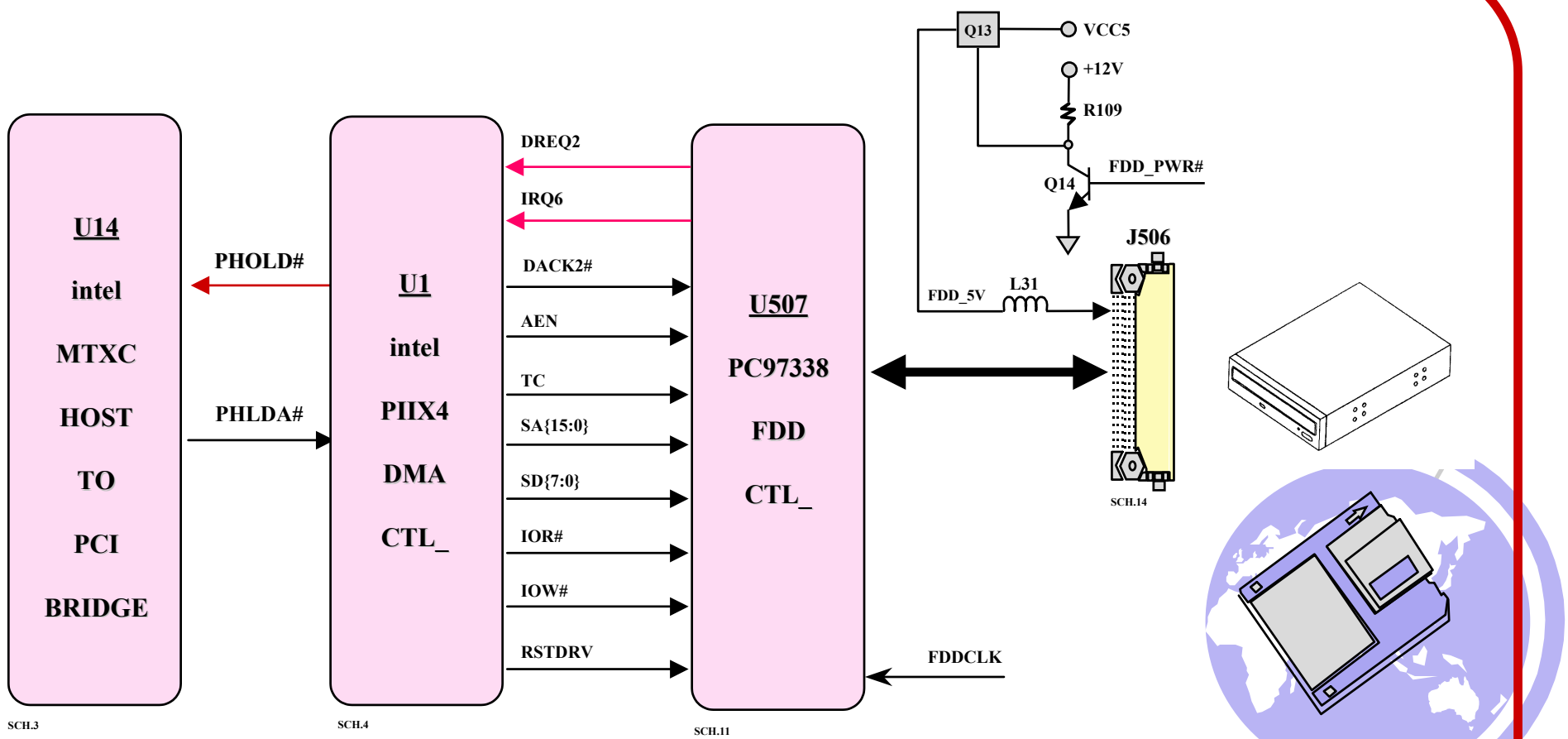
SYMPTOM:
AN ERROR MESSAGE IS SHOWN WHEN THE TOUCH-PAD IS ENABLED.



9.9 DISKETTE DRIVE TEST ERROR

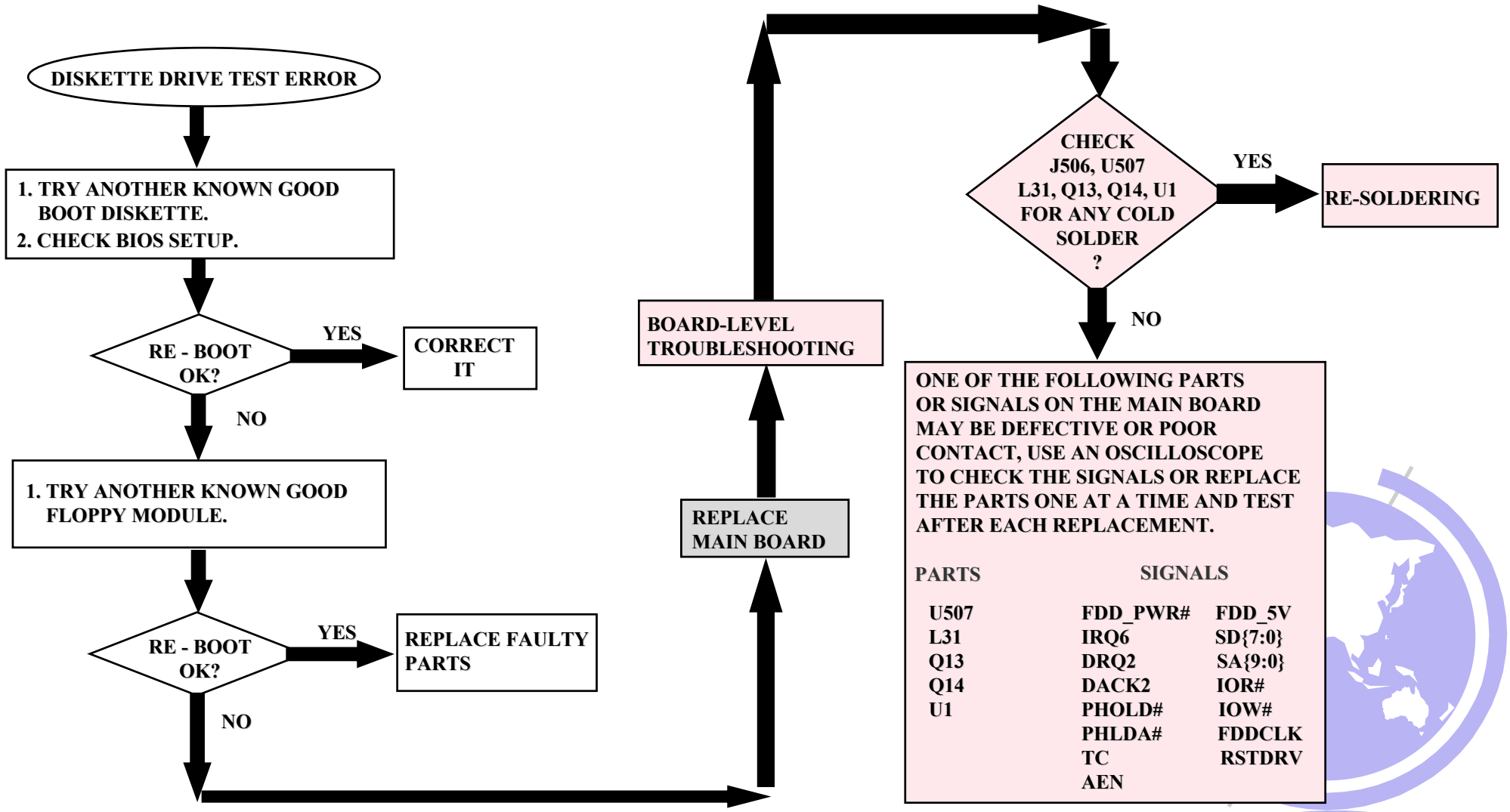
SYMPTOM:

AN ERROR MESSAGE IS SHOWN WHILE LOADING DATA FROM DISK TO SYSTEM.



9.9 DISKETTE DRIVE TEST ERROR

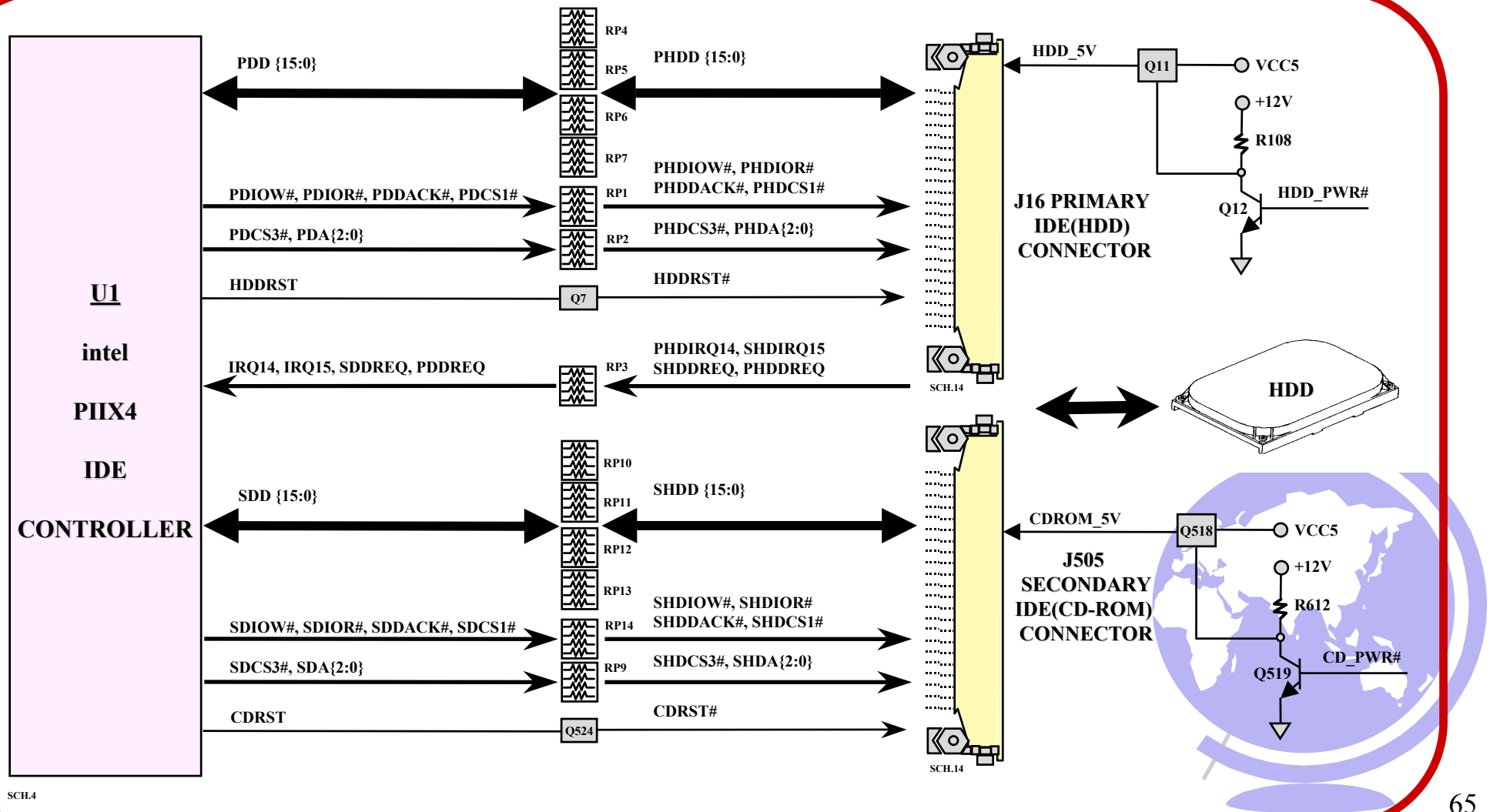
SYMPTOM:
AN ERROR MESSAGE IS SHOWN WHILE LOADING DATA FROM DISK TO SYSTEM.



9.10 HARD DRIVE TEST ERROR

SYMPTOM:

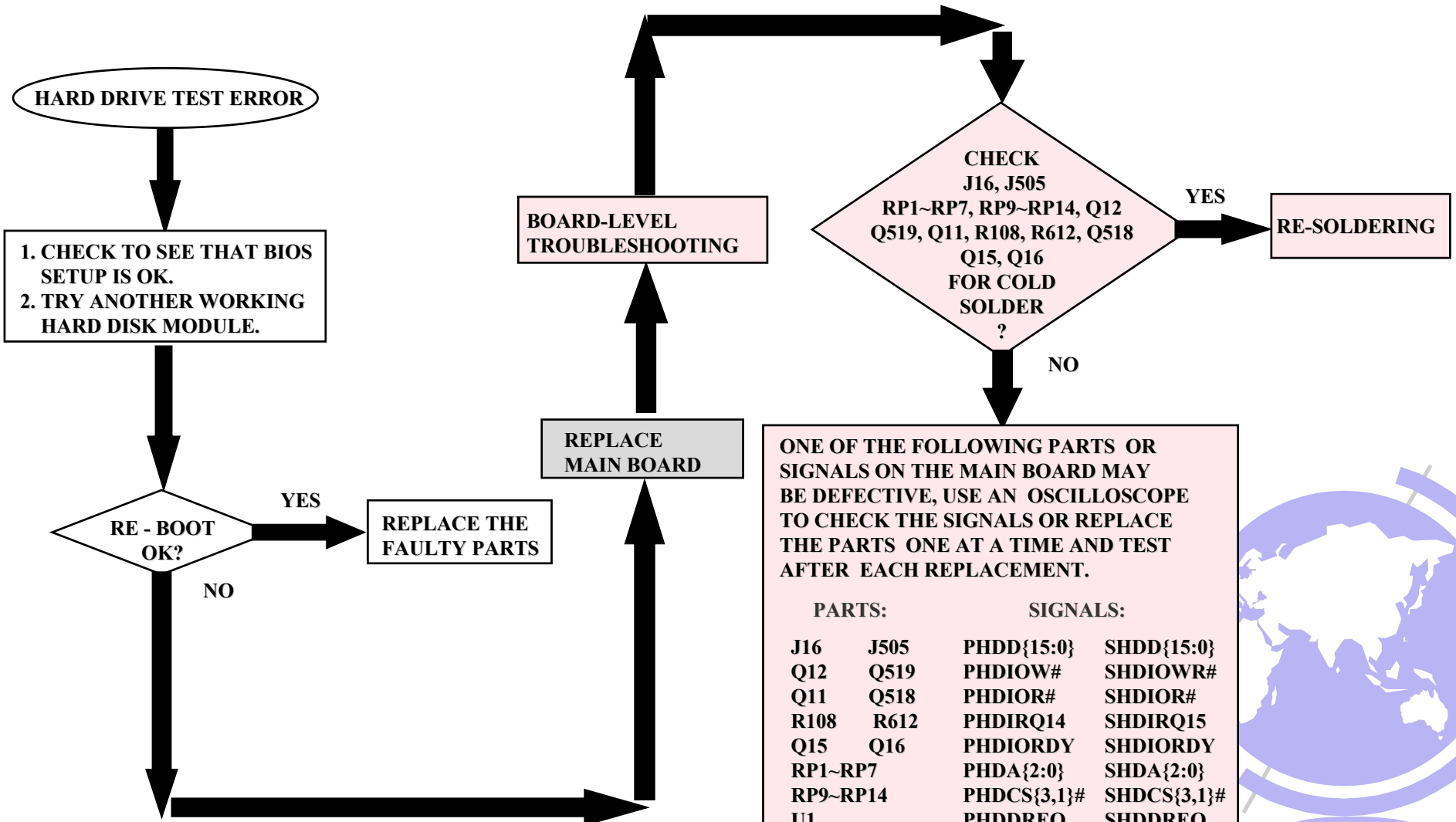
EITHER AN ERROR MESSAGE IS SHOWN, OR THE DRIVE MOTOR SPINS NON-STOP, WHILE READING DATA FROM OR WRITING DATA TO HARD-DISK.



9.10 HARD DRIVE TEST ERROR

SYMPTOM:

EITHER AN ERROR MESSAGE IS SHOWN, OR THE DRIVE MOTOR SPINS NON-STOP, WHILE READING DATA FROM OR WRITING DATA TO HARD-DISK.



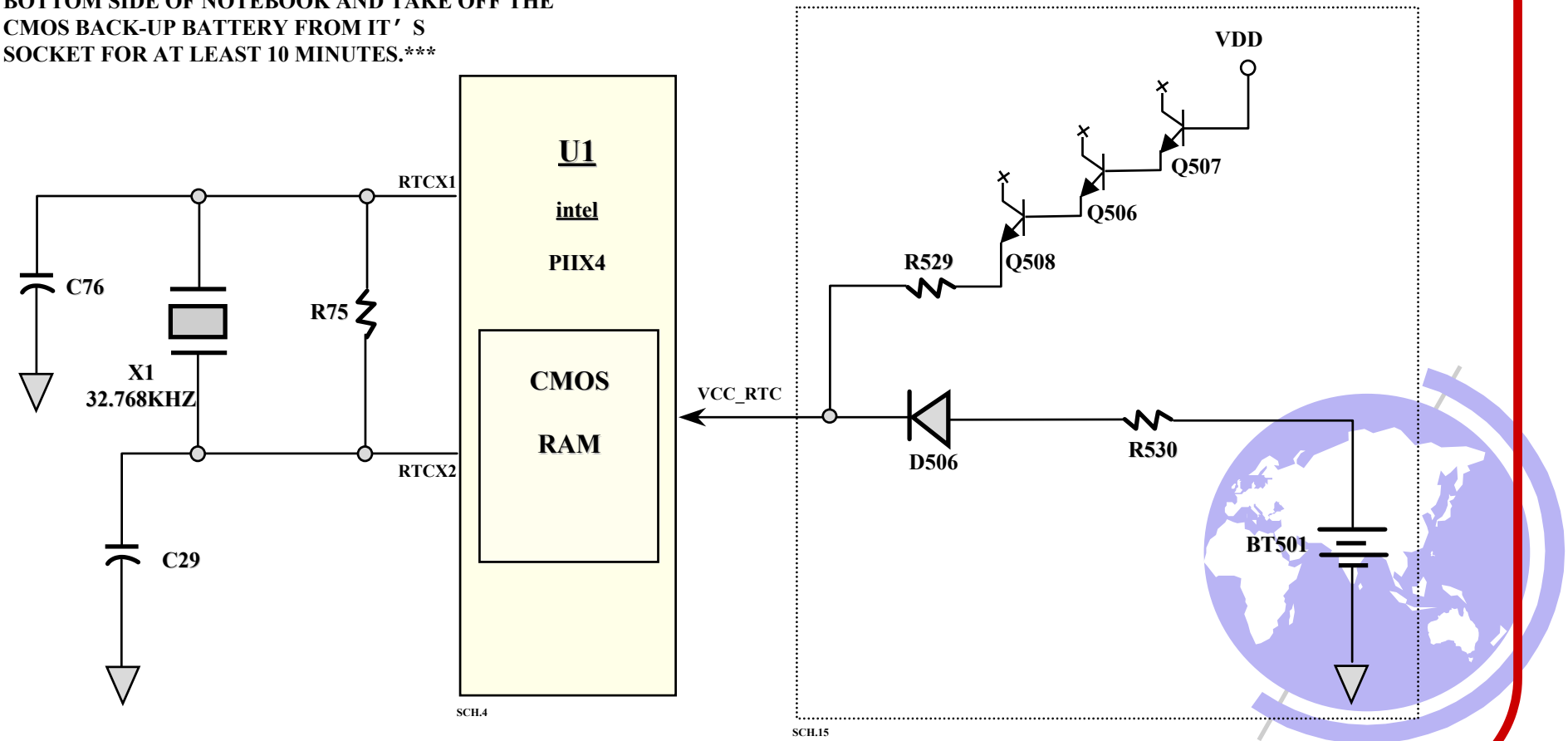
9.11 CMOS TEST ERROR

SYMPTOM:

1. ERROR CODE IS STOPEED AT 22H.

2. CMOS DATA LOST, OR INACCURATE SYSTEM TIME & DATE.

TO CLEAR CMOS DATA, REMOVE BATTERY PACK AND DISCONNECT AC ADAPTER FIRST, THEN REMOVE CMOS BATTERY COMPARTMENT COVER ON THE BOTTOM SIDE OF NOTEBOOK AND TAKE OFF THE CMOS BACK-UP BATTERY FROM IT' S SOCKET FOR AT LEAST 10 MINUTES.

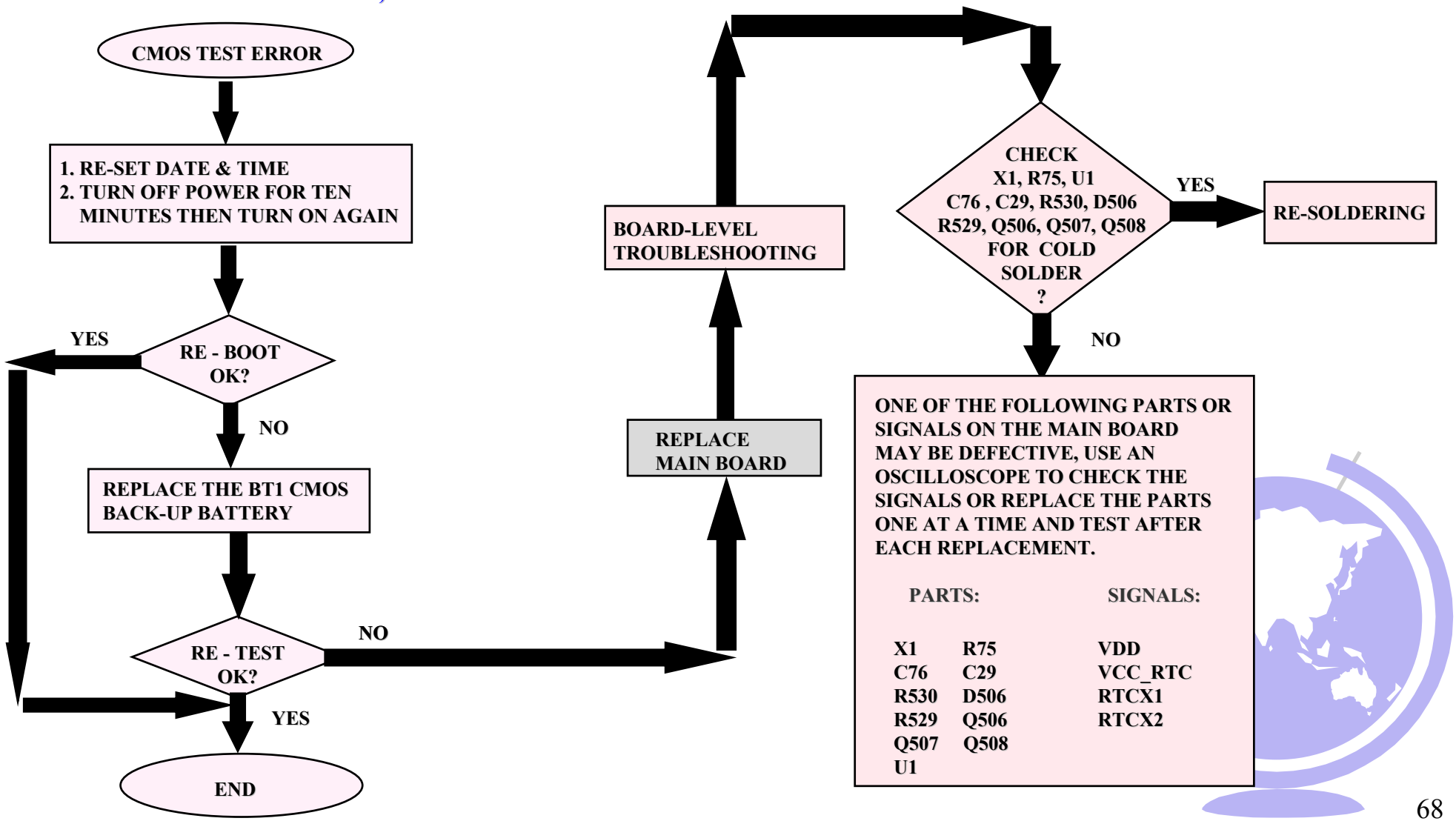


9.11 CMOS TEST ERROR

SYMPTOM:

1. ERROR CODE IS STOPEED AT 22H.

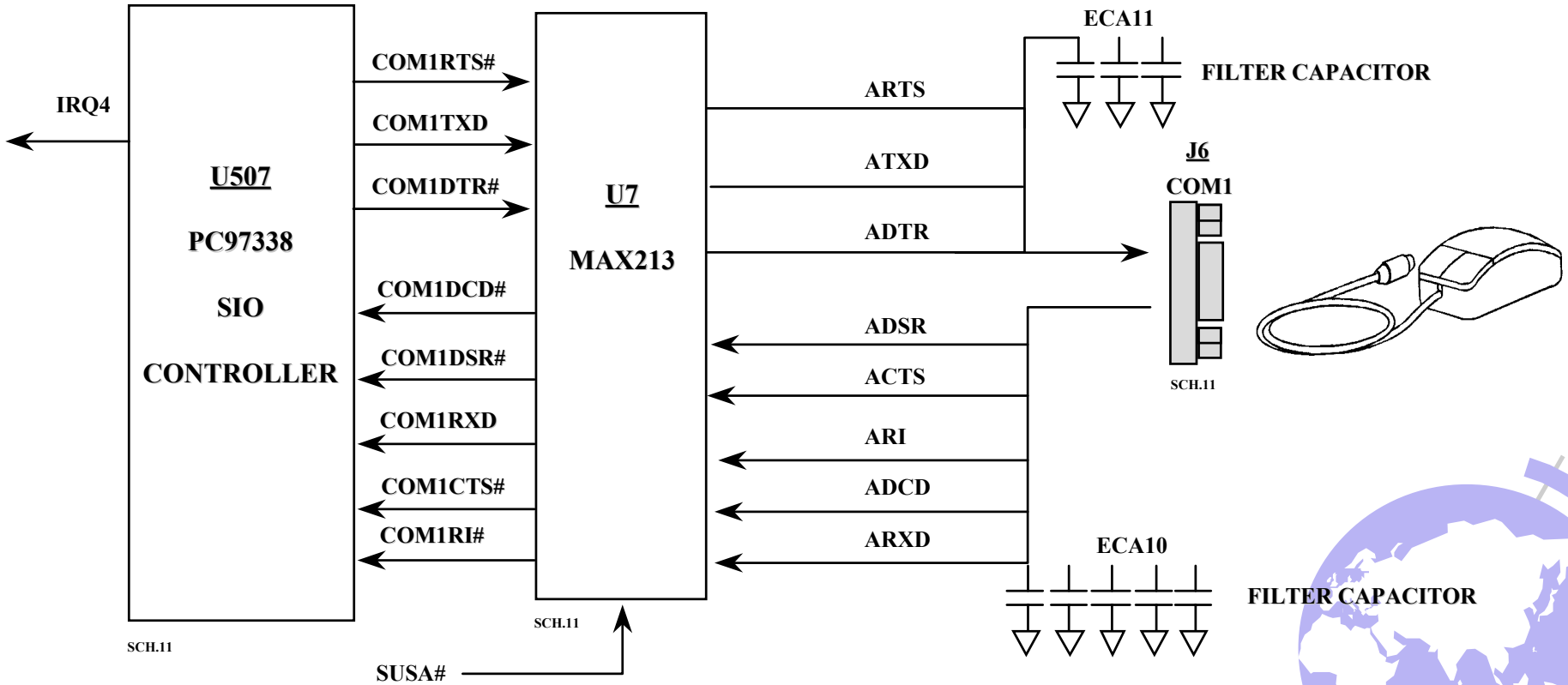
2. CMOS DATA LOST, OR INACCURATE SYSTEM TIME & DATE.



9.12 SIO PORT TEST ERROR

SYMPTON:

ERROR OCCURS WHEN A MOUSE OR OTHER I/O SERIAL DEVICE IS INSTALLED.



PIN DEFINITION OF SIO PORT:

PIN 1	DCD	DATA CARRIER DETECT	PIN 6	DSR	DATA SET READY
PIN 2	RD	RECEIVE DATA	PIN 7	RTS	REQUEST TO SEND
PIN 3	TD	TRANSMIT DATA	PIN 8	CTS	CLEAR TO SEND
PIN 4	DTR	DATA TERMINAL READY	PIN 9	RI	RING INDICATOR
PIN 5	SG	SIGNAL GROUND			

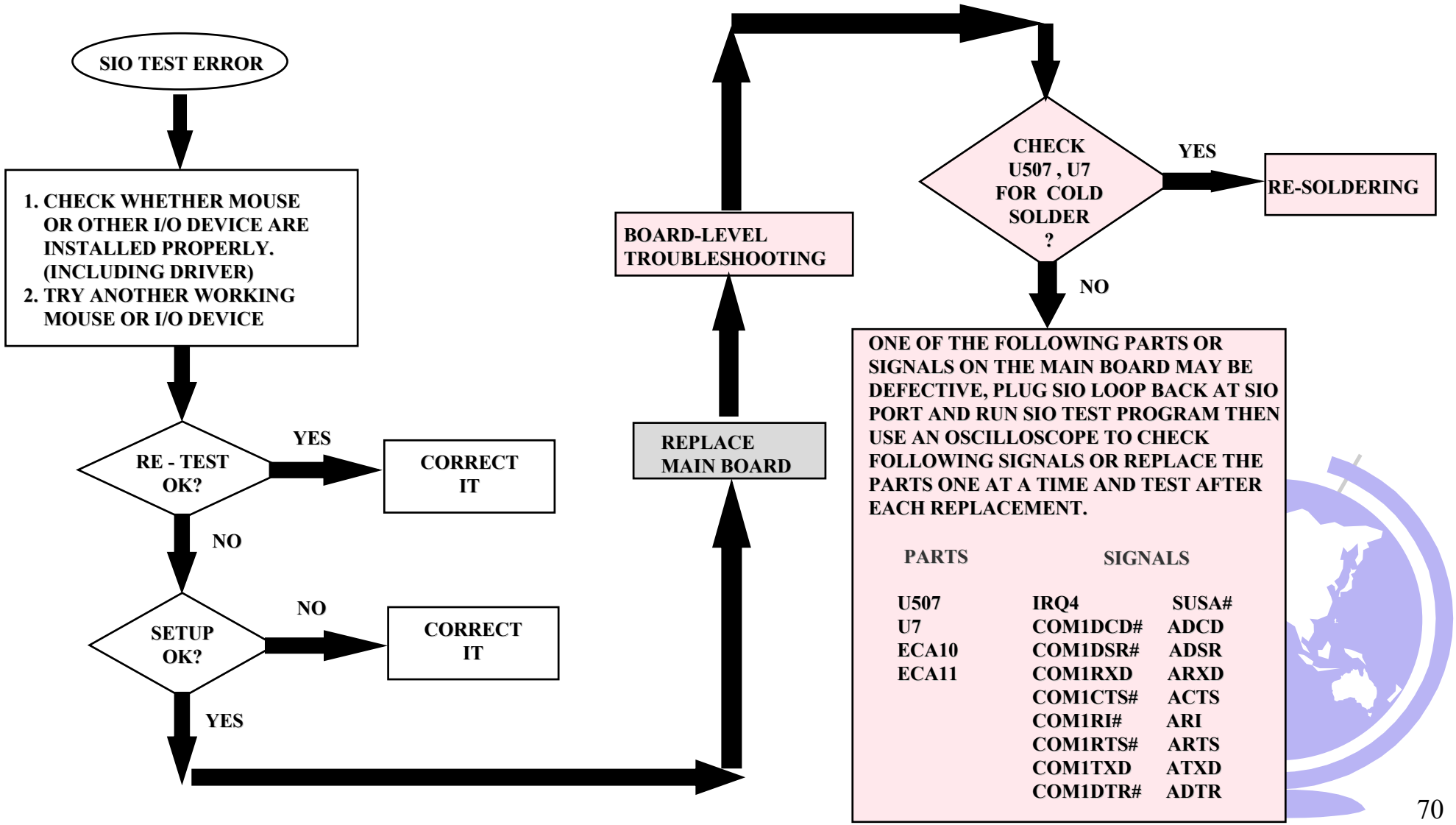
LOOPBACK CONNECTOR FOR SIO TEST:

PIN 1,4,6	SHORT
PIN 2,3	SHORT
PIN 7,8,9	SHORT

9.12 SIO PORT TEST ERROR

SYMPTON:

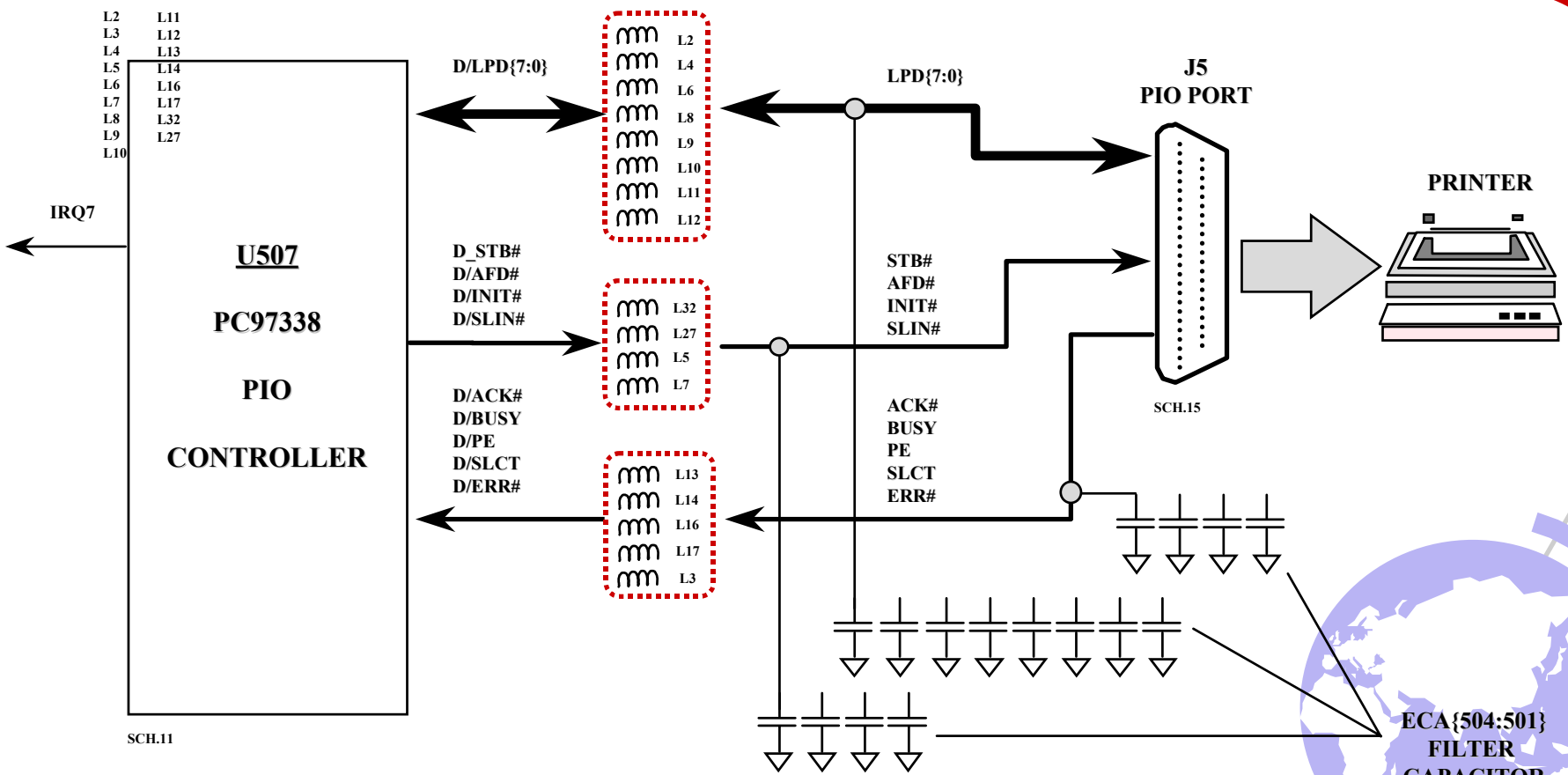
ERROR OCCURS WHEN A MOUSE OR OTHER I/O SERIAL DEVICE IS INSTALLED.



9.13 PIO PORT TEST ERROR

SYMPTON:

WHEN A PRINT COMMAND IS ISSUED, PRINTER PRINTS NOTHING OR GARBAGE.



PIN DEFINITION OF PIO PORT

PIN 1	STB	STROBE SIGNAL	PIN 14	AFD	AUTO LINE FEED
PIN 2-9	D0 -D7	PARALLEL PORT DATA BUS D0 TO D7	PIN 15	ERR	ERROR AT PRINTER
PIN 10	ACK	ACKNOW LEDGE HANDSHANK	PIN 16	INIT	INITIATE OUTPUT
PIN 11	BUSY	BUSY SIGNAL	PIN 17	SLIN	PRINTER SELECT
PIN 12	PE	PAPER END	PIN 18-25:		SIGNAL GROUND
PIN 13	SLCT	PRINTER SELECTED			

LOOPBACK CONNECTOR FOR PIO TEST:

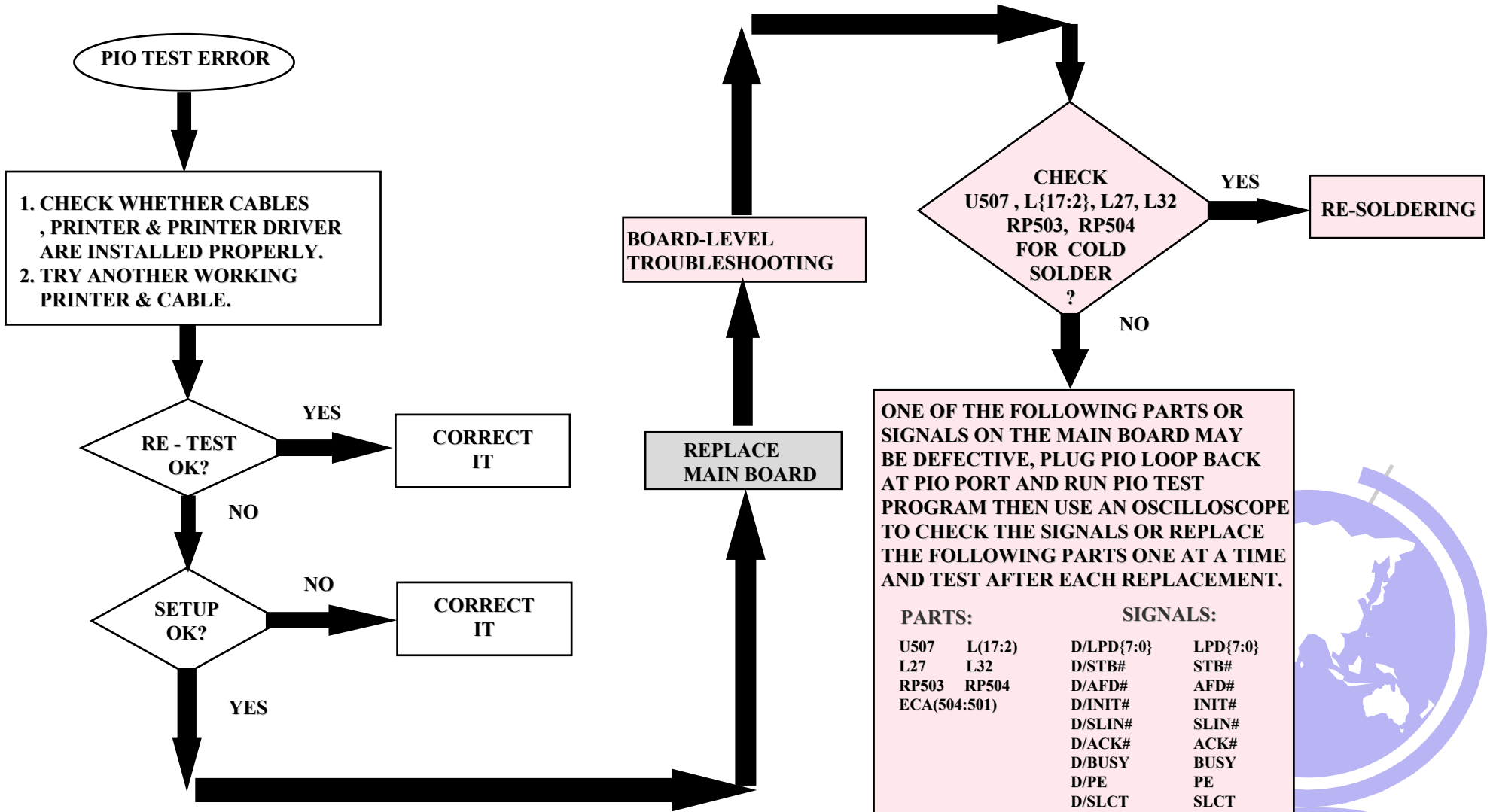
PIN 1,13	SHORT	PIN 10,16	SHORT
PIN 2,15	SHORT	PIN 11,17	SHORT
PIN 12,14	SHORT		

LOOPBACK CONNECTOR FOR EPP TEST:

PIN 1,2,4,6,8	SHORT
PIN 3,5,7,9,16	SHORT
PIN 18,19,20,21,22,23,24,25	SHORT

9.13 PIO PORT TEST ERROR

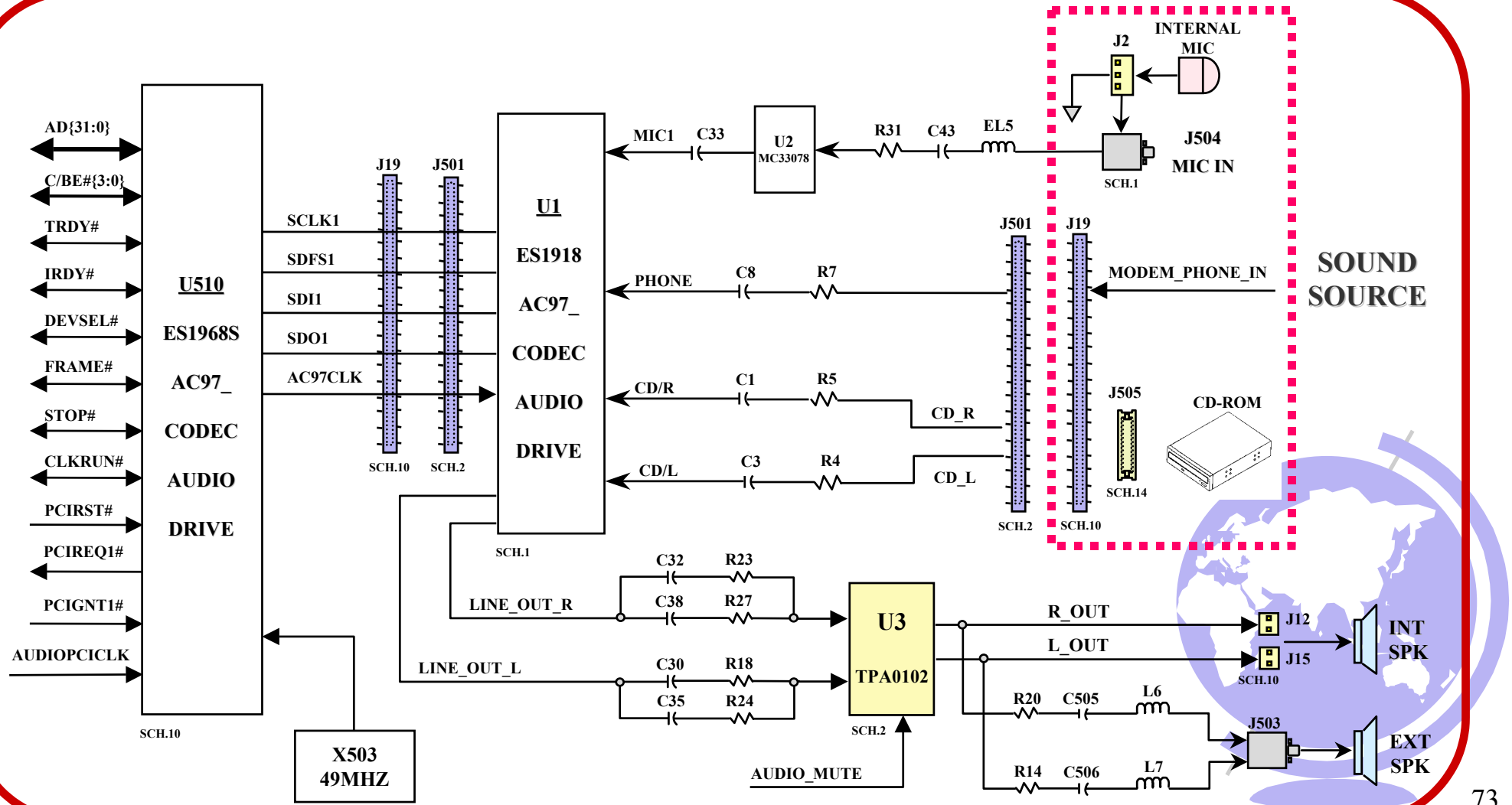
SYMPTON:
WHEN A PRINT COMMAND IS ISSUED, PRINTER PRINTS NOTHING OR GARBAGE.



9.14 AUDIO DRIVE FAILURE

SYMPTON:

NO SOUND FROM SPEAKER AFTER AUDIO DRIVE IS INSTALLED OR NO SOUND FROM CD-ROM, MICROPHONE AND MODEM VOICE.



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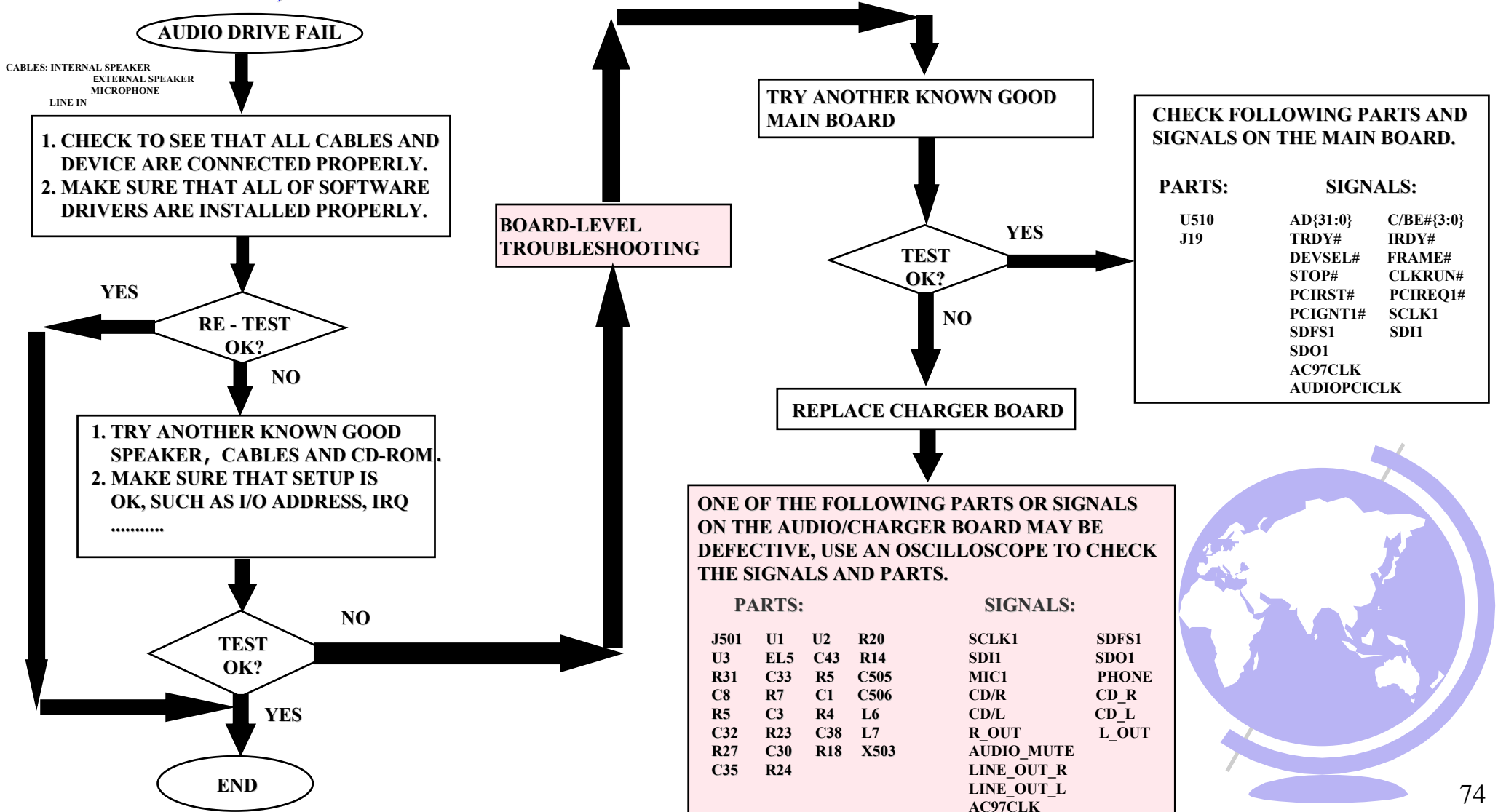
SYMPTON:

NO SOUND FROM SPEAKER AFTER AUDIO DRIVE IS INSTALLED OR NO SOUND FROM CD-ROM, MICROPHONE AND MODEM VOICE.

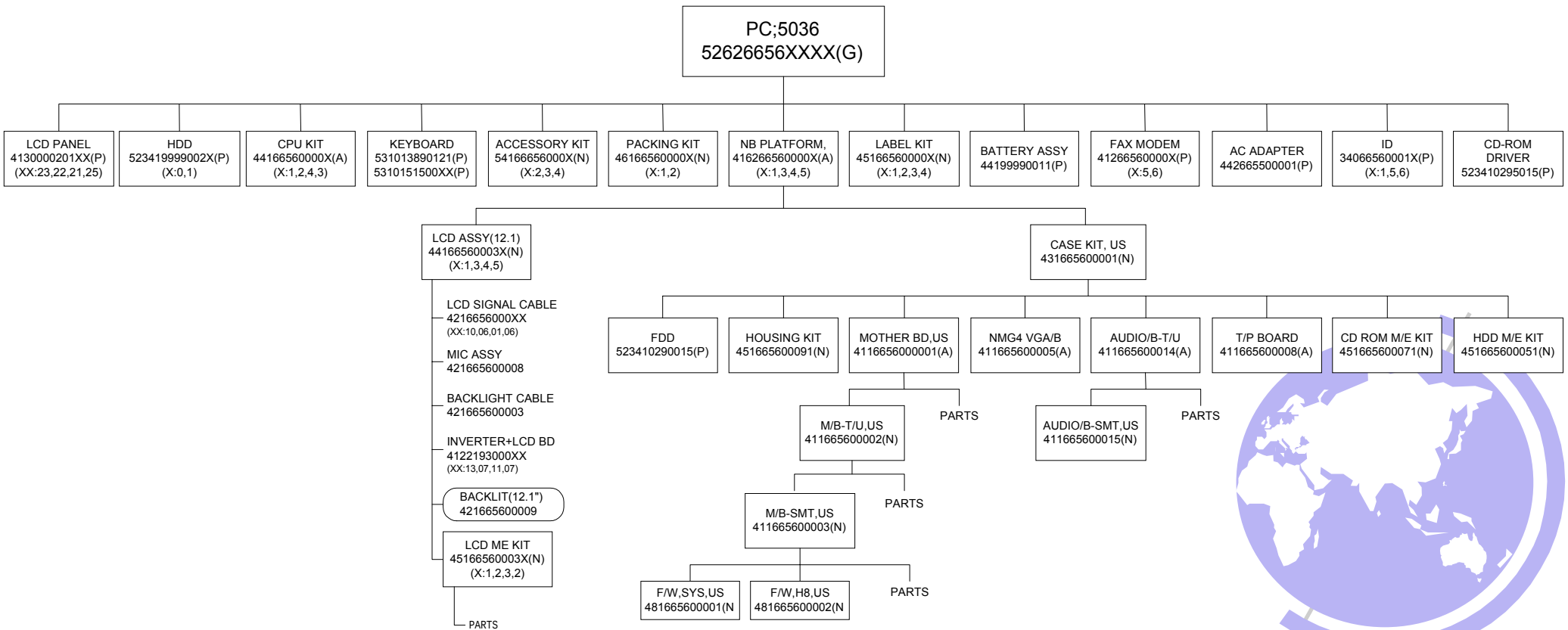


10. BOM TREE STRUCTURE

5036 BOM STRUCTURE (DETAIL)

PROJECT CODE: 738

REVISION:R03(08/01/98)



11. EXPLODED VIEWS

12. SPARE PARTS LIST(1)

PART_NO	DESCRIPTION	LOCATION
526266560010	NBX;5036/TSXA/XXA/XXX1/BXDB2	
413000020122	LCD;LT133X2-122,TFT,13.3",XGA,SA	
416266560003	NB PLATFORM;TFT,SAMSUNG,13.3,503	
412219300010	PCB ASSY;D/A BD,ONLY SAMSUNG,503	
421665600003	CABLE ASSY;BACKLIT TO M/B,5036	
421665600006	CABLE ASSY;LCD-VGA 13.3" SAM,503	
421665600031	MICROPHONE ASSY;5036	
340665600002	BEZEL ASSY;LCD 13.3",5036	
340665600005	HOUSING ASSY;LCD 13.3" SAMSUNG,5	
342665600001	HINGE;LCD,R,5036	
342665600002	HINGE;LCD,L,5036	
345665600004	HOLDER;MICROPHONE,5036	
345665600005	CUSHION;LCD BOTTOM,5036	
345665600006	CUSHION;LCD TOP,5036	
346665600002	INSULATOR;INV BD,5036	
371103030501	SCREW;M3L5,K-HEAD(+),NIB/NLK	
370102610602	SPC-SCREW;M2.6 L6,NIB,K-HD,727	
370102020301	SPC-SCREW;M2L3,NIW,K-HEAD	
346665200015	FILM;LCD PROTECT,13.3",215*290,P	
523410290015	FD DRIVE;1.44M,3 MODE,FD-05HG-56	
342665600006	BRACKET;I/O,5036	
344665600036	CAP;FAX/MODEM,5036	
340665600013	PLATE ASSY;KEYBOARD,5036	
344665600029	COVER;CD-ROM,FPC CABLE,5036	
344665600013	LENS;I/R,5036	
344665600033	KNOB;TOUCH PAD,5036	
344665600008	COVER;CABLE,5036	
344665600027	COVER;BIOS,5036	
344665600010	COVER;HINGE,5036	
344665600021	COVER;DRAM,5036	
332300000114	CABLE;FFC,4P,T/P,SW,5036	
332300000113	CABLE;FFC,8P,T/P,5036	

PART_NO	DESCRIPTION	LOCATION
340665600012	COVER ASSY;I/O,5036	
340665600007	TOP CASE ASSY;5036	
340665600010	BOTTOM CASE ASSY;5036	
346665600004	INSULATOR;FDD,5036	
371102030301	SCREW;M2L3,FLT(+),NIB/NLK	
371103031201	SCREW;M3L12,K-HEAD(+),NIB/NLK	
341665600005	SPRING PLATE;LCD CABLE,5036	
422665600001	FPC ASSY;FDD-M/B TEAC,5036	
421665600051	FAN ASSY;5036	
442110500007	TOUCH PAD MODULE;904251-0000,L65	
346665600014	SHIELD;AUDIO PCB,5036	
346665600015	MYLAR;DC-CONN,5036	
345665600001	RUBBER FOOT;5036	
370102631201	SPC-SCREW;M2.6L12,K-HEAD(+),NIB	
370102010301	SPC-SCREW;M2L3,NIB,B-HD,727	
346665600016	MYLAR;TOUCH PAD,5036	
346665600017	MYLAR;T/P SWITCH BD,5036	
377102650940	S-STANDOFF;M2.6DP4.3H9.4L4,NCG/N	
370102020301	SPC-SCREW;M2L3,NIW,K-HEAD	
371102030601	SCREW;M2L6,K-HEAD(+),NIB/NLK	
421664900062	CABLE ASSY;ESD TOUCH PAD,5027	
370102610602	SPC-SCREW;M2.6 L6,NIB,K-HD,727	
370103010801	SPC-SCREW;M3L8,NIB,K-HD,727	
345665600007	RUBBER FOOT;HDD CONN,5036	
411665600001	PWA;PWA-5036 MOTHER BD	
371102030801	SCREW;M2L8,FLT(+),NIB/NLK	
378102050491	STANDOFF;M2H4.9,NCG	
371102010601	SCREW;M2L6,FLT(+),NIW	
298000000002	BATTERY HOLDER;FOR CR2032,BH-800	BT501
312271006350	EC;100U ,25V,20%,RA,6.3*7,-40~10	PC10,13,11
312272206152	EC;220U ,4V ,M,RA,D8*5,OS-CON	PC3,19
312273306151	EC;330U ,6.3V,20%,RA,D10,W/OS-CO	PC16,17

12. SPARE PARTS LIST(2)

PART_NO	DESCRIPTION	LOCATION
313000020132	CHOKE;22UH/18.5T,.6D,55040,LIE	PL1
313001050040	XSFORMER;18U/17.5T/36.5T/.8D/.35	PL2
331510080001	CON;RBN,MA,80P,.63MM,R/A	J8
331720009004	CON;D,MA,9P,2.775,R/A	J6
331720015006	CON;D,FM,15P,2.29,R/A,3ROW	J4
331720025005	CON;D,FM,25P,2.775,R/A	J5
331870004002	CON;MINI DIN,4P,R/A,W/GROUNDING	J14
331870006011	CON;MINI DIN,6P,R/A,W/GROUNDING	J11
331910003003	CON;POWER JACK,3P,16VDC/3A	J13
338530010005	BATTERY;LI,3V/220MAH,CR2032	BT501
411665600003	PWA;PWA-5036 SMT V0 MOTHER BD	
271012000301	RES;0 ,1/8W,5% ,1206,SMT	R535
271045107101	RES;.01 ,1W ,1% ,2512,SMT	PR509,511
271045257101	RES;.025 ,1W ,1% ,2512,SMT	PR503
271071000002	RES;0 ,1/16W,0603,SMT	R18,19,23
271071100302	RES;10 ,1/16W,5% ,0603,SMT	R39,84,14,126
271071101301	RES;100 ,1/16W,5% ,0603,SMT	R101,82
271071102302	RES;1K ,1/16W,5% ,0603,SMT	R45,566,585,
271071103302	RES;10K ,1/16W,5% ,0603,SMT	R30,33,61,
271071104101	RES;100K ,1/16W,1% ,0603,SMT	PR5,R26,37,63,81,
271071124311	RES;124K ,1/16W,1% ,0603,SMT	PR502,513
271071105101	RES;1M ,1/16W,1% ,0603,SMT	R75,118
271071153301	RES;15K ,1/16W,5% ,0603,SMT	R7,8,11,16
271071204101	RES;200K ,1/16W,1% ,0603,SMT	PR9
271071221302	RES;22 ,1/16W,5% ,0603,SMT	R9,10,62,77,539,
271071222302	RES;2.2K ,1/16W,5% ,0603,SMT	R587
271071270301	RES;27 ,1/16W,5% ,0603,SMT	R5,R6
271071330302	RES;33 ,1/16W,5% ,0603,SMT	R530,547-549,554,556
271071470301	RES;47 ,1/16W,5% ,0603,SMT	R570,571,574,576
271071471302	RES;470 ,1/16W,5% ,0603,SMT	R80,99
271071472302	RES;4.7K ,1/16W,5% ,0603,SMT	R21,34,584,3,48
271071473301	RES;47K ,1/16W,5% ,0603,SMT	R41

PART_NO	DESCRIPTION	LOCATION
271071474301	RES;470K ,1/16W,5% ,0603,SMT	PR7,R65
271071514301	RES;510K ,1/16W,5% ,0603,SMT	PR517
271071562301	RES;5.6K ,1/16W,5% ,0603,SMT	R567,R1
271071564301	RES;560K ,1/16W,5% ,0603,SMT	R501,608
271071682101	RES;6.8K ,1/16W,1% ,0603,SMT	R95
271071750101	RES;75 ,1/16W,1% ,0603,SMT	R42,44,60,512,513
271071909211	RES;90.9K,1/16W,1% ,0603,SMT	PR516
271611100301	RP;10*4 ,8P ,1/16W,5% ,0612,SMT	RP25-29,32-35
271611103301	RP;10K*4 ,8P ,1/16W,5% ,0612,SMT	RP38,45,501
271611220301	RP;22*4 ,8P ,1/16W,5% ,0612,SMT	RP1,2,4-7,9-14
271611222301	RP;2.2K*4,8P ,1/16W,5% ,0612,SMT	RP44
271611472301	RP;4.7K*4,8P ,1/16W,5% ,0612,SMT	RP503,511
271611820301	RP;82*4 ,8P ,1/16W,5% ,0612,SMT	RP3
271621102303	RP;1K*8 ,10P,1/16W,5% ,1206,SMT	RP22,504
271621103303	RP;10K*8 ,10P,1/16W,5% ,1206,SMT	RP8,16,36,506,15
271621472303	RP;4.7K*8,10P,1/16W,5% ,1206,SMT	RP18,19,24,30,31,39
271621473301	RP;47K*8 ,10P,1/16W,5% ,1206,SMT	RP37,40,17,20,21
272003104701	CAP;.1U ,CR,25V ,+80-20%,0805,Y	PC511
272002105701	CAP;1U ,CR,16V ,-20+80%,0805,SM	C60,79,86,PC508
272012225702	CAP;2.2U ,CR,16V ,+80-20%,1206,Y	C27,33,37,543,562
272012335701	CAP;3.3U ,CR,16V ,-20+80%,1206,S	C509
272012475701	CAP;4.7U ,CR,16V ,+80-20%,1206,Y	C20,97,106,529,611
272013105501	CAP;1U ,CR,25V ,+80-20%,1206,S	PC505
272021106501	CAP;10U ,10V ,20%,1210,X7R,SMT	PC504,516,519
272043106501	CAP;10U ,CR,25V ,20%,1812,Y5U,S	PC512
272063226701	CAP;22U ,25V ,+80-20%,2220,Y5U,	C582,581
272073180401	CAP;18P ,CR,25V ,10%,0603,NPO,S	C29,76,623
272075100401	CAP;10P ,50V ,10%,0603,COG,SMT	EC33,C553,554
272072104702	CAP;.1U ,16V,+80-20%,0603,SMT	C6,PC7,C8-10,21,22
272075101701	CAP;100P ,50V ,+80-20%,0603,SMT	EC30,C25,624
272075102701	CAP;1000P,50V ,+80-20%,0603,SMT	PC1,EC22,519,C570
272075103501	CAP;.01U ,50V ,20%,0603,SMT	EC24,C59,19,501,502

12. SPARE PARTS LIST(3)

PART_NO	DESCRIPTION	LOCATION
272075104701	CAP;.1U ,50V,+80-20%,0603,SMT	PC4,502,506,507,
272075181301	CAP;180P ,50V ,5% ,0603,SMT	EC15,518,541,540
272075221302	CAP;220P ,50V ,5% ,0603,SMT	EC23,25
272075470401	CAP;47P ,50V ,10%,0603,COG,SMT	PC14
272075472701	CAP;4700P,50V ,+80-20%,0603,SMT	C622
272022106501	CAP;10U ,16V,20%,1210,Y5U,SMT	PC6,509,C41,100,506
273000010003	FERRITE CHIP;36OHM/100MHZ,4332	L506,PL501-503
273000110015	FERRITE CHIP;80OHM/100MHZ,3216,3	L31,510,29,24,EL3
273000130006	FERRITE CHIP;600OHM/100MHZ,.2A,1	L18,19
273000130010	FERRITE CHIP;130OHM/100MHZ,1608,	EL1,2,4-8,501-504
273000150002	FERRIET CHIP;120OHM/100MHZ,2012,	L501,502,511,
273000990012	INDUCTOR;10UH,CDRH127,SUMIDA,SMT	PL3
274011431404	XTAL;14.318MHZ,30PPM,32PF,SMT	X501
274011600405	XTAL;16MHZ,30PPM,16PF,SMT	X502
274013276103	XTAL;32.768KHZ,30PPM,12.5PF,CM20	X1
282074338401	IC;74CBT3384DBQ,Q SWITCH,QSOP,24	U17
282574014004	IC;74AHC14,HEX INVERTER,TSSOP,14	U6
282574032005	IC;74AHC32,QUAD 2-I/P OR,TSSOP,1	U18
282574164002	IC;74VHC164,SIPO REGISTER,TSSOP,	U10
283766560001	IC;SDRAM,1M*16*4-100,TSOP,54P,50	U8,9,504,505
284100430001	IC;FW82439TX,MTXC,CPU/PCI,BGA,32	U14
284182371005	IC;FW82371EB,PIIX4E,PCI/ISA,BGA3	U1
284501220001	IC;PCI1220,PCI/CARDBUS,TQFP,208P	U5
284501968001	IC;ES1968S,AUDIO CHIP,TQFP,100P	U510
481665600002	F/W ASSY;KBD CTRL,5036	U511
284583434001	IC;H8/F3434,KBD CTLR,TQFP,100P	
242600000145	LABEL;10*10,BLANK,COMMON	
284597338001	IC;PC97338VJG,SUPER I/O,TQFP,100	U507
286200213002	IC;ADM213E,RS-232,+-15KVESD,SSOP	U7
286300809002	IC;MAX809,RESET CIRCUIT,2.9V,SOT	U15
286302206001	IC;TPS2206,CARDBUS PWR CTLR,SSOP	U11

PART_NO	DESCRIPTION	LOCATION
286303032001	IC;SB3032P,PWM CTLR,SO,16P	PU501
286303052001	IC;SB3052P,PWM CTRL,SSOP,28P	PU1
286317812001	IC;HA178L12UA,VOLT REGULATOR,SC-	PU502
284504867001	IC;W48S67-02,SYSTEM CLOCK,SSOP,4	U509
288031110001	FIR;IBM31T1100A,TRANSCE. MODULE,	U12
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	PD1-3
288100056001	DIODE;RLZ5.6B,ZENER,5.6V,5%,LL34	PD504
288100202001	DIODE;DAN202K,80V,SWITCH,SMT	PD4,PD6
288100212001	DIODE;DAN212K,80V,SWITCH,SOT23	D3,505,506,510
288100701002	DIODE;BAV70LT1,70V,225MW,SOT-23	D5,518
288101004024	DIODE;EC10QS04,RECT,40V,1A,CHIP,	PD501-503
288104148001	DIODE;RLS4148,200MA,500MW,MELF,S	D502,515
288200352001	TRANS;NDS352P,DMOS,TO-236AB	Q2,6,528
288200144001	TRANS;DTC144WK,NPN,SMT	Q1,7,4,501,3
288203904010	TRANS;MMBT3904L,NPN,Tr35NS,TO236	PQ4,Q5,506-508
288204410001	TRANS;SI4410DY,N-MOSFET,.02OHM,S	PQ2,3,501-504
291000012006	CON;HDR,MA,10P*2,1MM,ST,SMT	J1
291000011205	CON;HDR,FM,60P*2,.8MM,ST,SMT	J2
291000015010	CON;HDR,FM,25P*2,.65MM,H3MM,ST,S	J16,505,3
291000016012	CON;HDR,FM,30P*2,1.27MM,H4.2,ST,	J19
291000018301	CON;HDR,FM,83P,1.27MM,ST,SMT	J502,503
291000142604	CON;FPC/FFC,26P,1MM,ST,SMT,MOLEX	J18
291000410201	CON;WFR,MA,2P,1.25,ST,SMT/MB	J12,15,20
291000410301	CON;WFR,MA,3P,1.25,ST,SMT/MB	J9
242600000158	LABEL;10*10,BLANK,COMMON,HI-TEMP	
283420402003	IC;FLASH,256K*8-120,5V,PLCC32,BT	
291000621448	DIMM SOCKET;144P,.8MM,H5.6,SMT	J501
291000622802	DIMM SOCKET;280P,.6MM,FM,COPPER,	J17
297040105003	SW;PUSU BUTTON,SPST,12V/50MA,4P,	SW1
271023918301	RES;9.1 ,1/4W,5% ,1210,SMT	R46,47
288100056003	DIODE;BAW56,70V,215MA,SOT-23	D501

12. SPARE PARTS LIST(4)

PART NO	DESCRIPTION	LOCATION
271071103101	RES;10K ,1/16W,1% ,0603,SMT	PR514
274014915401	XTAL;49.152MHZ,50PPM,18PF,SMT	X503
288227002001	TRANS;2N7002LT1,N-CHANNEL FET	Q15,Q16,Q20
288202302001	TRANS;SI2302DS,N-MOSFET,SOT-23	Q13,11,518
273000500010	CHOKE COIL;500IHM/100MHZ,5036,SM	T1
295000010016	FUSE;NORMAL,6.5A/32VDC,3216,SMT	F2
295000010008	FUSE;1.1A,POLY SWITCH,SMT	F501,502,1,503
291000142002	CON;FPC/FFC,20P,1MM,ST,52610-209	J506
272602107501	EC;100U,16V,M,6.3*5.5,-55+85'C,S	C504,505
272615470401	CP;47P*4 ,8P,50V ,10%,0612,NPO,	ECA14,15,12
272613103401	CP;.01U*4 ,8P,25V ,10%,0612,X7R,	ECA13
272615101401	CP;100P*4 ,8P,50V ,10%,0612,NPO,	ECA10,11,3
272615181401	CP;180P*4 ,8P,50V ,10%,0612,NPO,	ECA501,502,503,504
272615221401	CP;220P*4 ,8P,50V ,10%,0612,NPO,	ECA4,5
282574008005	IC;74AHC08,QUAD 2-I/P AND,TSSOP,	U19
271071226311	RES;226K ,1/16W,1% ,0603,SMT	PR6
272075220701	CAP;22P ,50V ,+80-20%,0603,SMT	C605,609,626
288100073002	DIODE;SFPJ-73,DC2010,30V,3A,SMT	PD5
271071184101	RES;180K ,1/16W,1% ,0603,SMT	R119
288202301001	TRANS;SI2301DS,P-MOSFET,SOT-23	Q533
286302951015	IC;LP2951ACM,VOLTAGE REGULATOR,S	U512
273000150103	INDUCTOR;.82UH,150mA,2012,SMT	L513
272073152401	CAP;1500P,CR,25V ,10%,0603,X7R,S	C629
331000004007	CON;USB,MA,R/A,4P*1,3505-04NBT1S	J7
371102030301	SCREW;M2L3,FLT(+),NIB/NLK	
346665600005	INSULATOR;CARDBUS,5036	
344600000217	IC CARD CON PART;83P,H5.8MM,CARD	
225664300001	TAPE;INSULATION,AC04,5024	
346665400032	WASHER;PCMCIA/CAR BOX,VENUS	
242600000195	LABEL;PENTIUM-BP,SYSTEMSOFT BIOS	
411665600005	PWA;PWA-5036 VGA BD NMG4	

PART NO	DESCRIPTION	LOCATION
271071000002	RES;0 ,1/16W,0603,SMT	R10,14
271071100302	RES;10 ,1/16W,5% ,0603,SMT	R6,518
271071102302	RES;1K ,1/16W,5% ,0603,SMT	R513,21
271071103302	RES;10K ,1/16W,5% ,0603,SMT	R4,5,17,506,503
271071105101	RES;1M ,1/16W,1% ,0603,SMT	R509,2
271071113101	RES;11K ,1/16W,1% ,0603,SMT	R508
271071221302	RES;22 ,1/16W,5% ,0603,SMT	R13,19,517,523
271071224301	RES;220K ,1/16W,5% ,0603,SMT	R505
271071330302	RES;33 ,1/16W,5% ,0603,SMT	R512,514-515,28,29
271071680301	RES;68 ,1/16W,5% ,0603,SMT	R526-527,516
271071750101	RES;75 ,1/16W,1% ,0603,SMT	R7,8,18,20,22,23,26
271611330301	RP;33*4 ,8P ,1/16W,5% ,0612,SMT	RP1-4
272002105701	CAP;1U ,CR,16V ,-20+80%,0805,SM	C13,15,18,22-23,
272022106501	CAP;10U ,16V,20%,1210,Y5U,SMT	C2,35,503,506,508,
272012475701	CAP;4.7U ,CR,16V ,+80-20%,1206,Y	C38,534,535
272022106701	CAP;10U ,16V,+80-20%,1210,Y5V,S	C26,28,511
272072104702	CAP;.1U ,16V,+80-20%,0603,SMT	C6,24,27,30,32,34,
272073180401	CAP;18P ,CR,25V ,10%,0603,NPO,S	C5,12
272075103702	CAP;.01U ,50V,+80-20%,0603,SMT	C17,20,33,36,39,514
273000010003	FERRITE CHIP;36OHM/100MHZ,4332	L1
273000130012	FERRITE CHIP;70OHM/100MHZ,1608,S	L501,EL501,
273000150002	FERRIET CHIP;120OHM/100MHZ,2012,	L506,508
274011431405	XTAL;14.318MHZ,20PPM,18PF,SMT	X1
284500725001	IC;AD725,RGB TO NTSC/PAL,SO,16P	U501
284502160001	IC;NM2160,VGA CTRL,TQFP,176P	U3
284505330001	IC;PI5V330,WIDEBAND/VIDEO,QSOP,1	U5
284507584001	IC;SN75LVDS84,LVDS18BIT,SSOP48,5	U4
286501410001	IC;MK1410,NTSC/PAL CLOCK,SO,8P,S	U503
288200144001	TRANS;DTC144WK,NPN,SMT	Q501
288209410001	TRANS;SI9410DY,N-MOSFET,.04OHM,S	Q1
288227002001	TRANS;2N7002LT1,N-CHANNEL FET	Q502

12. SPARE PARTS LIST(5)

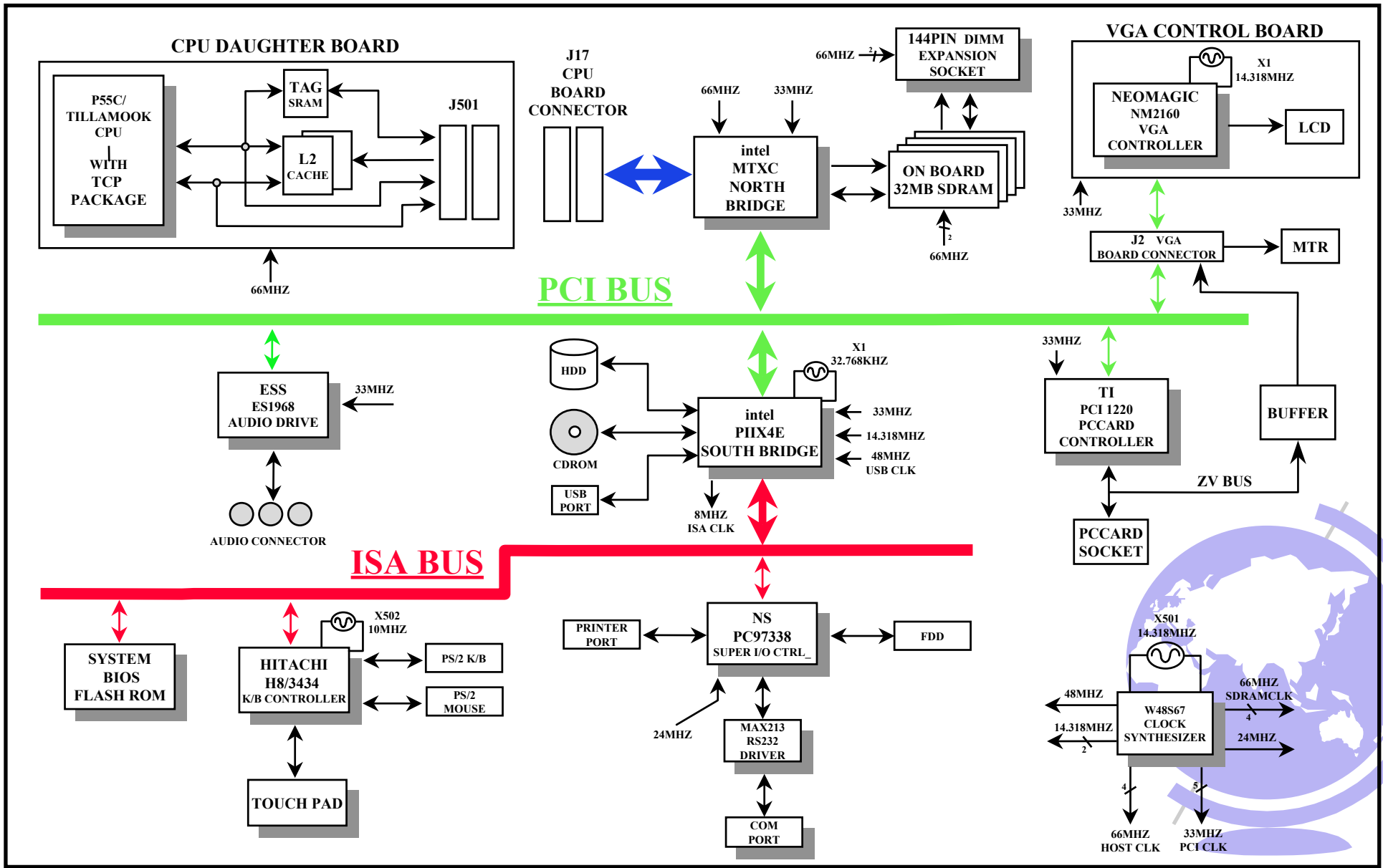
291000011204	CON;HDR,MA,60P*2,.8MM,ST,SMT	J501
291000012101	CON;HDR,MA,21P,0.625MM,ST,SMT	J3
291000410203	CON;WFR,MA,2P,1.25MM,ST,SMT,HIRO	J2
297040105004	SW;PUSH BUTTON,4P,12VDC/50MA,TM0	SW1
271002000301	RES;0 ,1/10W,5%,0805,SMT	R511,522,525,L2
286303480001	IC;LM3480,VOLTAGE REGULATOR,SOT-	U505
411665600014	PWA;PWA-5036 T/U V0B AUDIO CHAR	
312271006350	EC;100U,25V,20%,RA,6.3*7,-40~10	PC510,511
313000020132	CHOKE;22UH/18.5T,.6D,55040,LIE	PL502
331030006006	CON;HDR,MA,6P*1,2.0,ST,GLD	J502
331840005006	CON;STEREO JACK,5P,R/A,W9.1,MOJB	J504,503
271002472301	RES;4.7K ,1/10W,5%,0805,SMT	PR512
271012000301	RES;0 ,1/8W,5%,1206,SMT	AL1
271012278101	RES;2.7 ,1/8W,1%,1206,SMT	R12
271045257101	RES;.025 ,1W,1%,2512,SMT	PR1
271071000002	RES;0 ,1/16W,0603,SMT	R1,2,4,5,7,10,13
271071101301	RES;100 ,1/16W,5%,0603,SMT	R501
271071102102	RES;1K ,1/16W,1%,0603,SMT	PR2
271071103101	RES;10K ,1/16W,1%,0603,SMT	PR3,4,R18,23,24
271071104101	RES;100K,1/16W,1%,0603,SMT	R32-35,PR5-7,12,510
271071105101	RES;1M ,1/16W,1%,0603,SMT	PR10,14,15
271071121211	RES;12.1K,1/16W,1%,0603,SMT	PR8
271071122301	RES;1.2K ,1/16W,5%,0603,SMT	R8
271071131101	RES;130 ,1/16W,1%,0603,SMT	PR504
271071153301	RES;15K ,1/16W,5%,0603,SMT	R25,26
271071154101	RES;150K,1/16W,1%,0603,SMT	PR506
271071203101	RES;20K ,1/16W,1%,0603,SMT	R22,19,PR509
271071205311	RES;205K,1/16W,1%,0603,SMT	PR501
271071221302	RES;22 ,1/16W,5%,0603,SMT	R11,504
271071222302	RES;2.2K ,1/16W,5%,0603,SMT	R29,9
271071473301	RES;47K ,1/16W,5%,0603,SMT	R30
271071287311	RES;287K ,1/16W,1%,0603,SMT	PR513
271071301311	RES;301K ,1/16W,1%,0603,SMT	PR511
271071333301	RES;33K ,1/16W,5%,0603,SMT	PR13,R17,28
271071471302	RES;470 ,1/16W,5%,0603,SMT	R16
271071472302	RES;4.7K ,1/16W,5%,0603,SMT	R36-38
271071499111	RES;4.99K,1/16W,1%,0603,SMT	PR508,PR507
271071562311	RES;562K ,1/16W,1%,0603,SMT	PR505.11
271071593101	RES;59K ,1/16W,1%,0603,SMT	PR503
271071682101	RES;6.8K ,1/16W,1%,0603,SMT	R3,6,31
271071753101	RES;75K ,1/16W,1%,0603,SMT	PR515
271071887211	RES;88.7K,1/16W,1%,0603,SMT	PR502
271071976211	RES;97.6K,1/16W,1%,0603,SMT	PR9
271611102301	RP;1K*4 ,8P ,1/16W,5%,0612,SMT	RP1
272002105701	CAP;1U ,CR,16V ,-20+80%,0805,SM	C1-11,13,29,30
272012225702	CAP;2.2U,CR,16V ,+80-20%,1206,Y	C28
272022106701	CAP;10U ,16V,+80-20%,1210,Y5V,S	C14,18,23,27,31,PC5
272041226501	CAP;22U ,CR,10V ,20%,1812,X7R,S	C15,39
272063226501	CAP;22U ,25V ,20%,2220,Y5U,SMT	PC9,14
272072104702	CAP;.1U ,16V,+80-20%,0603,SMT	PC8,10,11,C12,16,17
272073180401	CAP;18P ,CR,25V ,10%,0603,NPO,S	C22,503
272075100701	CAP;10P ,50V ,+80-20%,0603,SMT	PC2
272075101701	CAP;100P ,50V ,+80-20%,0603,SMT	EC2,PC3,EC3,PC13,C48
272075102701	CAP;1000P,50V ,+80-20%,0603,SMT	C19,20,36
272075562401	CAP;5600P,CR,50V ,10%,0603,X7R	PC4
272075103702	CAP;.01U ,50V,+80-20%,0603,SMT	C41,42,501
272075104701	CAP;.1U ,50V,+80-20%,0603,SMT	PC1,6,7,12,16
272075390301	CAP;39P ,50V ,5%,0603,NPO,SMT	PC503
272075471401	CAP;470P ,50V,10%,0603,SMT	C40
272602227502	EC;220U ,16V,M,6.3*7.7,-15+105',	C506,505
272615470401	CP;47P*4 ,8P,50V ,10%,0612,NPO,	ECA501
273000130006	FERRITE CHIP;600OHM/100MHZ,.2A,1	L6,7,EL5-7,L501-3

12. SPARE PARTS LIST(6)

273000130010	FERRITE CHIP;130OHM/100MHZ,1608,	L1,504
273000130013	FERRITE CHIP;30OHM/100MHZ,1608	PL1,2,3,EL1,2,L4
273000150013	FERRITE CHIP;120OHM/100MHZ,2012,	L2,5,PL501
284501918001	IC;ES1918,AC 97 CODE,TQFP,48P	U1
286100102001	IC;TPA0102,AUDIO AMP,1.5W,TSSOP,	U3
286100393004	IC;LMV393,DUAL COMPARTOR,SSOP,8P	PU2
286101620001	IC;LT1620CS8,CURRENT SENSE AMP,S	PU1
286133078001	IC;MC33078D,LOW NOISE OP AMP.,SO	U2
286300431004	IC;AIC431,.5%,ADJ SHUNT REG,SOT-	PQ5
286301435001	IC;LTC1435CS,SW REG. CTRL,SO,16	PU501
288100018002	DIODE;RLZ18B,ZENER,18V,LL34,SMT	PD1
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	PD501
288100073002	DIODE;SFPJ-73,DC2010,30V,3A,SMT	PD502-504
288200144001	TRANS;DTC144WK,NPN,SMT	PQ4,501,502,Q1
288204410001	TRANS;SI4410DY,N-MOSFET,.02OHM,S	PQ1,2
288204435001	TRANS;SI4435DY,P-MOSFET,.035OHM,	PQ503
288227002001	TRANS;2N7002LT1,N-CHANNEL FET	PQ6,3
291000016011	CON;HDR,MA,30P*2,1.27MM,H6.8,ST,	J501
291000150403	CON;FPC/FFC,4P,1MM,R/A,SMT,MOLEX	J1
291000150805	CON;FPC/FFC,8P,1MM,R/A,SMT,MOLEX	J3
294011200001	LED;GRN,H1.5,0805,PG1102W,SMT	D1-D4
295000010016	FUSE;NORMAL,6.5A/32VDC,3216,SMT	PF501
271071402211	RES;40.2K,1/16W,1% ,0603,SMT	PR16
273000150009	FERRITE CHIP;30OHM/100MHZ,2012,S	L9
312272205352	EC;22U ,25V,20%,RA,6.3*5,LSM,85	PC501
411665600008	PWA;PWA-5036 T/P SWITCH BD	
291000140401	CON;FPC/FFC,4P,1MM,ST,NON-ZIF,SM	J1
297040102002	SW;PUSH BUTTON,SPST,15V/20MA,H3.	SW1,SW2
342665600005	BRACKET;CD-ROM,TEAC,5036	
422665600002	FPC ASSY;CD-ROM TEAC,5036	
346665600003	INSULATOR;CD ROM,5036	
332810000033	PWR CORD;125V/7A,2P,BLACK,AMERIC	

370102010201	SPC-SCREW;M2L2,NIW,K-HD,727	
340665600003	BEZEL ASSY;CD-ROM TEAC,5036	
346665600025	GASKET;FDD,5036	
370103010401	SPC-SCREW;M3L4,K-HD(+),D5.2,NIW,	
412665600003	PCB ASSY;HDD CONN. BD,5036	
370102010301	SPC-SCREW;M2L3,NIB,B-HD,727	
346665600012	GASKET;HDD,5036	
345665600007	RUBBER FOOT;HDD CONN,5036	
340665600014	BRACKET ASSY;HDD,5036	
221665120004	CARTON;AK/CARRYING BAG,N-B,5031	
227665600001	END CAP;5036	
222664820005	PE BAG;310*450,T.08,PITCHING	
220665600002	CARRYING BAG;N-B,5036	
221664750003	PARTITION;KEYBOARD,5026	
222664720004	PE BUBBLE BAG;KEYBOARD,5026	
222663920008	PE BAG;150*200,FRU,LP486	
222664220002	PE BAG;150*50,FRU,RECYCLE,LEBOOK	
222600020049	PE BAG;50*70MM,W/SEAL,COMMON	
242600000157	LABEL;BAR CODE & S/N,13.5*75,COM	
221664950002	PARTITION;CARRYING BAG,5027	
242662300009	LABEL;25*10MM,3020F	
242664400003	LABEL;WINDOWS 95,5023	
242665600001	LABEL;AGENCY-GLOBAL,5036	
343664710002	NAMEPLATE;LOGO,1,5026,N-B	
442665600002	BATT ASSY;14.8V/3.2AH,LI,TSB,503	
442665500001	AC ADPT ASSY;5033	
340665600011	COVER ASSY;KEYBOARD,5036	
523410295015	CD ROM DRIVE;24X,CD-224E-903,TEA	
222600050108	ENVELOPE;3.5" FD,PVC,COMMON	
242661900008	LABEL;3.5",EN,ALL COMMON	
551103200013	FLOPPY DISKETTE;3.5",1.44MB,2HD	

13. SYSTEM BLOCK DIAGRAM & SCHEMATICS



13. SYSTEM BLOCK DIAGRAM & SCHEMATICS

MOTHER-BOARD AUDIO/CHARGER BOARD

VGA-BOARD

52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74

75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96

97 98 99 100 101 102 103 104 105 106 107 108 109 110 111 112 113

114 115 116 117 118 119 120 121 122 123 124 125 125 127 128 129 130

13. SYSTEM BLOCK DIAGRAM & SCHEMATISS

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13. SYSTEM BLOCK DIAGRAM & SCHEMATISS

MOTHER-BOATD

DC /DC BOARD

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MOTHER-BOATD

DC /DC BOARD